ECMA
EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-102

RATE ADAPTATION FOR THE SUPPORT OF SYNCHRONOUS AND ASYNCHRONOUS EQUIPMENT USING THE V. SERIES TYPE INTERFACE ON A PCSN

Second Edition – July 1987

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BRIEF HISTORY

This Standard ECMA-102 is one of a series of standards for the connection of data processing equipment to private circuit switching networks.

It uses ISDN concepts as developed by CCITT and it is also within the framework of standards for Open Systems Interconnection as defined by ISO 7498 and within the Technical Report ECMA TR/25. It is based on the practical experience of ECMA Member Companies and the results of their active and continuous participation in the work of ISO, CCITT and various national standardization bodies in Europe and the USA. It represents a pragmatic and widely based consensus.

This Standard ECMA-102 specifies the rate adaptation scheme used by a terminal adaptor. It does not fully define all the functions of a terminal adaptor. Where appropriate, assumptions of the interface as presented by the private circuit switching network are also indicated.

This Second Edition of Standard ECMA-102 clarifies and provides explanatory text for a number of details which will ease implementation of the Standard (Appendix A refers).

Accepted as 2nd Edition of Standard ECMA-102 by the General Assembly of ECMA on 25 June 1987.

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1. GENERAL

1.1 Scope

This ECMA Standard defines the rate adaptation method used by terminal adaptors operating in accordance with circuit switching or leased circuit services which support an asynchronous or synchronous V.-Series interface.

This Standard is based upon CCITT Rec. I.463 (V.110), and uses the asynchronous-to-synchronous conversion technique described in CCITT Rec. V.22.

A major goal of this Standard is to achieve the maximum compatibility with CCITT Rec. I.463.

This Standard specifies:

- bit rate adaptation of asynchronous and synchronous user data,
- end-to-end synchronization of entry to, and exit from, the data transfer phase,
- provisions for network-independent clocking to allow the transfer of user data between two non-synchronized networks,
- provisions for flow control between terminal adaptors to allow the connection of two asynchronous terminals running at different data rates,
- provisions for performance monitoring.

1.2 Conformance

Conformance with this Standard implies satisfying all the requirements of Clauses 5, 6 and 7.

Implementation of network-independent clocking requires conformance with Clause 8.

Implementation of flow control for asynchronous DPEs requires conformance with Clause 9.

Implementation of performance monitoring requires conformance with Clause 11.

2. REFERENCES

ECMA-6	: 7-bit coded character set
CCITT Rec. I.461 (X.30)	: Support of X.21 and X.21bis based DTEs on the ISDN
CCITT Rec. I.463 (V.110)	: Support of DTEs with V.-Series type interfaces by an ISDN
CCITT Rec. V.5	: Standardization of data signalling rates for synchronous transmission in the general switched telephone network
CCITT Rec. V.6	: Standardization of data signalling rates for synchronous data transmission on leased telephone-type circuits

CCITT Rec. V.22	: 1200 bits per second duplex modem standardized for use on the general switched telephone network and on leased circuits
CCITT Rec. V.24	: List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment
CCITT Rec. V.25	: Automatic calling and/or answering equipment on the general switched telephone network, including disabling of echo suppressors on manually established calls
CCITT Rec. V.25bis	: Automatic calling and/or answering equipment on the general switched telephone network, using the 100 series interchange circuits
CCITT Rec. X.1	: International user classes of service in public data networks
CCITT Rec. X.21	: Interface between data terminal equipment and data circuit-terminating equipment for synchronous operation on public data networks
CCITT Rec. X.21bis	: Use on public data networks of data terminal equipment which is designed for interfacing to synchronous V.-Series modems.

3. DEFINITIONS AND ACRONYMS

For the purpose of this Standard the following definitions apply.

3.1 B-Channel

A 64 kbit/s duplex bearer channel with bit and octet timing. It is used to carry user data between TEs connected over a PCSN.

3.2 CSPDN

Circuit Switched Public Data Network.

3.3 Data Processing Equipment (DPE)

Specific type of terminal exclusively or mainly used to process data (in contrast to voice only terminal equipment).

3.4 ISDN

Integrated Services Digital Network.

3.5 InterWorking Unit (IWU)

The equipment needed to allow interworking between a PCSN and another network.

3.6 Private Circuit Switching Network (PCSN)

A circuit switching network with full digital transmission capabilities bounded by S interfaces.

3.7 PSTN

Public Switched Telephone Network.

3.8 Terminal Adaptor (TA)

A set of terminal adaptation functions. It allows Terminal Equipment with V.-Series or X.-Series interfaces to be connected to a PCSN. The TA may extract the information required for rate adaptation from the in-band coding and/or from signalling when required.

3.9 Terminal Equipment (TE)

Any terminal (voice or data processing) connected to a PCSN at the S reference point.

3.10 TE-1

Terminal Equipment operating at the S reference point, incorporating signalling functions.

3.11 TE-2

Data processing equipment (DPE) with a V.- or X.-Series interface.

3.12 Universal Terminal Adaptor

A TA capable of supporting various asynchronous and synchronous user data rates including at least the recommended basic set of speeds specified in this Standard.

4. REFERENCE CONFIGURATIONS

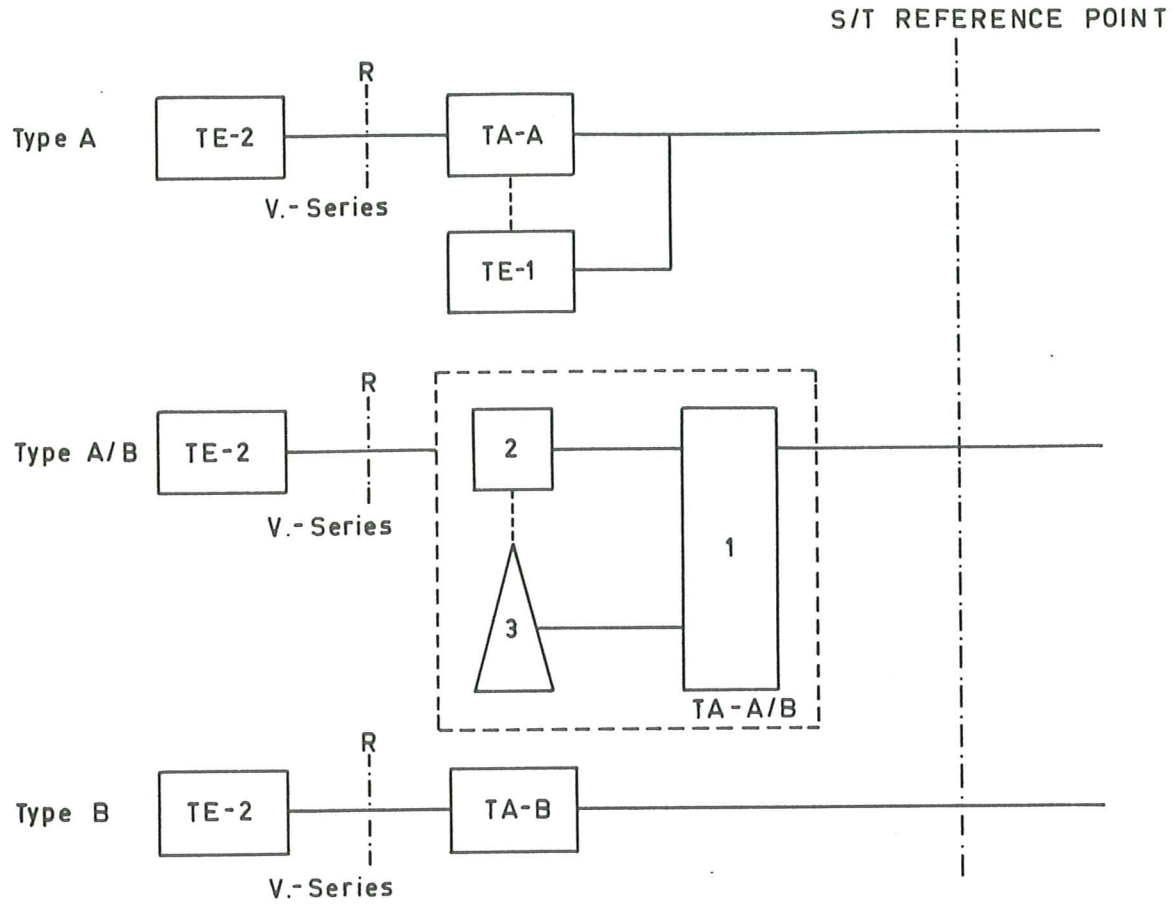
Figures 1 and 2 show examples of some of the many possible functional groupings. These figures are included simply as an aid to describing the rate adaptation method in later Clauses.

4.1 Customer Access Configuration

Figure 1 shows several possible functional groupings that could be used for the connection of DPEs with V.-Series type interfaces to a PCSN.

Note 1

The connection of modems to the analogue side of the A/D converter in the TE-1 functional grouping (e.g. a digital telephone) is not addressed in this Standard. Whilst this type of connection may be useful to users, and is allowed, it is not the subject of this Standard.



1 = Common TE-1 and TA functions (e.g. S interface)
2 = Specific TA-A functions (e.g. data rate adaptation)
3 = Specific TE-1 functions (e.g. signalling)

Figure 1 - Customer Access - Reference Connection

4.1.1 TA-A Functions

The TA-A provides manual call control functions associated with an alternate voice/data, circuit switching service. The following functions are included:

i) Conversion of the electrical and mechanical, functional and procedural characteristics of the V.-Series type interface(s) to those required by a PCSN at reference point S.

ii) Bit rate adaptation of V.-Series data signalling rates to 64 kbit/s B channel rate as described in Clause 5.

iii) End-to-End synchronization of entry to, and exit from, the data transfer phase as described in Clause 7.

The TA-A does not include signalling functions.

4.1.2 TA-A/B Functions

TA-A/B is a TA which combines TA-A and TE-1 functions.

4.1.3 TA-B Functions

The TA-B provides in addition to those functions provided by a TA-A, the mapping functions necessary to convert automatic calling and/or automatic answering procedures to the signalling protocols used by a PCSN. CCITT Rec. V.25 and Rec. V.25bis provide examples of such protocols.

4.1.4 TA-X

The TA-X is a TA which supports an X.-Series interface.

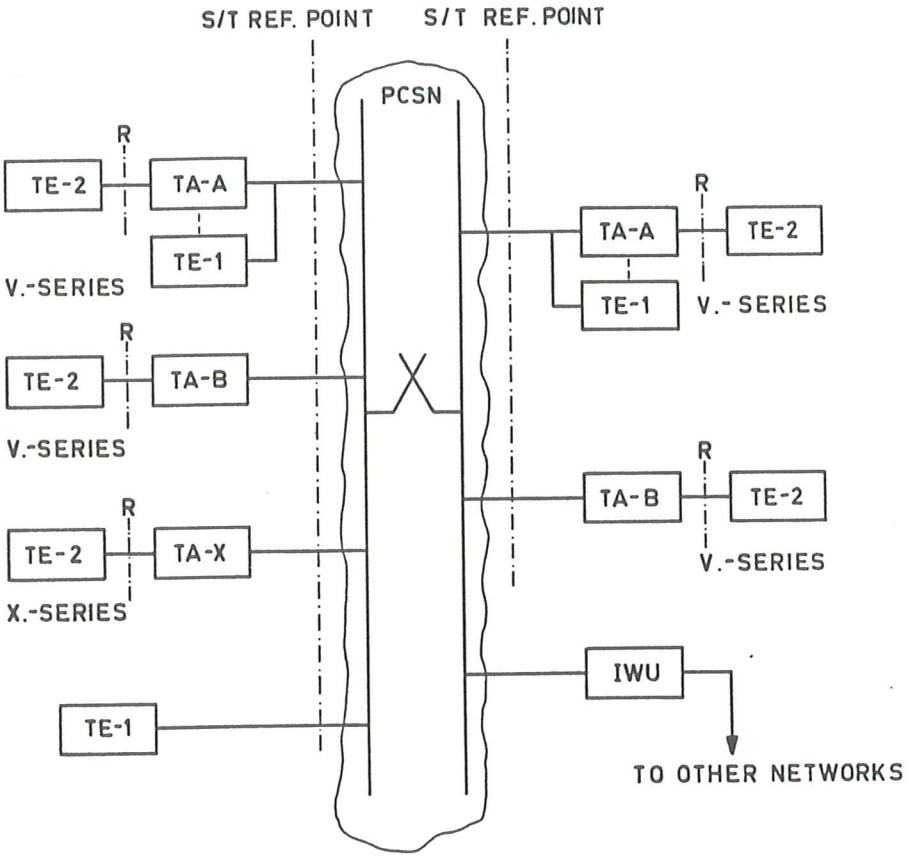


Figure 2 - Network Reference Configurations

4.2 Types of End-to-End Connections

The terminal adaptor functions described in this Standard take into account the end-to-end connection types shown in Figure 2. The figure shows the inter-operation cases considered in this Recommendation, as follows:

i) V.-Series TE-2 with V.-Series TE-2,

ii) V.-Series TE-2 with X.21 TE-2.

Interworking with TEs on other networks is considered in Clause 10.

Interworking with other networks may also be provided on the basis of trunk interconnection using Interworking Units (IWUs). Use of an IWU is outside the scope of this Standard.

5. BIT RATE ADAPTATION

5.1 General Approach

The bit rate adaptation functions within the TA are shown in Figure 3. A three-stage methods is employed, with functional blocks RA0, RA1 and RA2. Function RA0 is an asynchronous-to-synchronous conversion-stage, using the technique defined in CCITT Rec. V.22 for the support of the basic signalling rate range, and is not used on synchronous user data. It produces a synchronous stream defined by 2^n times 600 bit/s (where n = 0 to 5). Function RA1 converts the user data signalling rate or stream from RA0 to an appropriate intermediate rate defined by 2^k times 8 kbit/s (where k = 0, 1 or 2). RA2 performs the final conversion from the intermediate rates generated by RA1 to 64 kbit/s. Synchronous data signalling rates of 48 kbit/s and 56 kbit/s are converted directly into the 64 kbit/s channel rate, and are considered in 5.5.

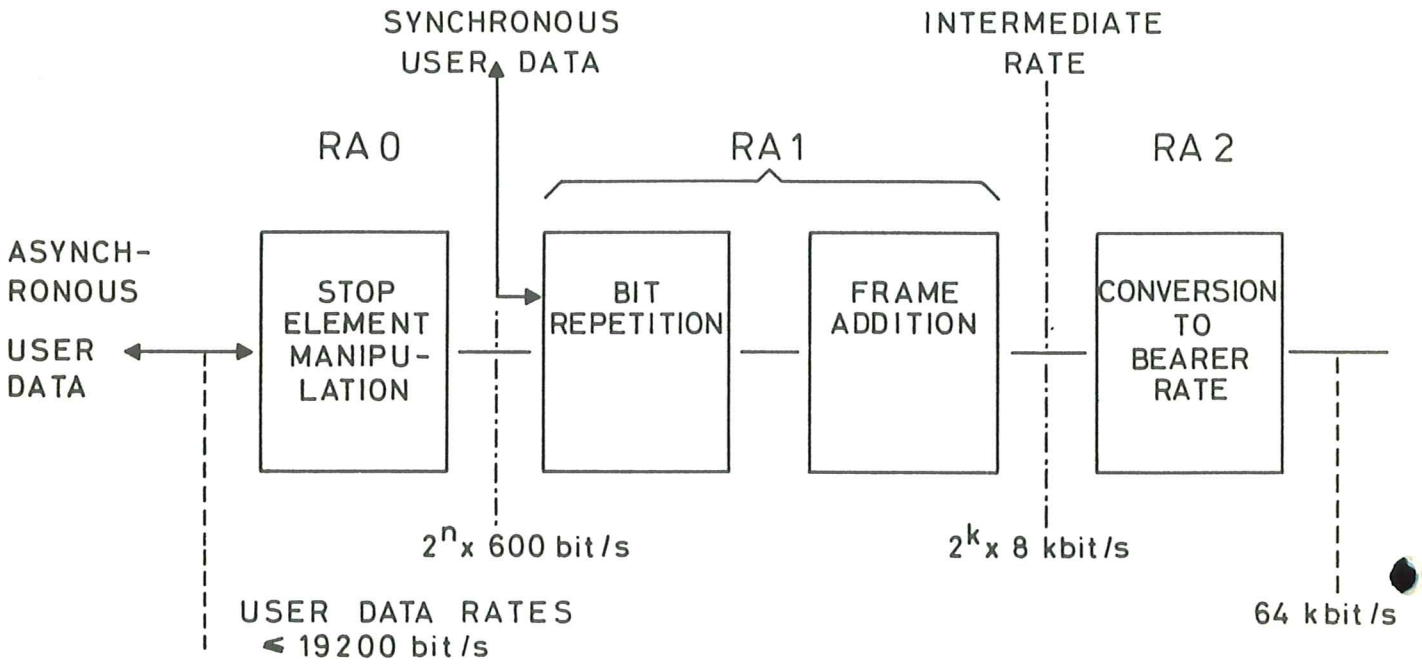


Figure 3 - Bit Rate Adaptation

5.1.1 User Rates

Data Rate bit/s		Intermediate Rate kbit/s
600	*	8
1200	*	8
2400	*	8
4800	*	8
7200		16
9600	*	16
14400		32
19200	*	32
48000		**
56000		**

Table 1 - Supported Synchronous User Rates

Note 2

* indicates mandatory support by a Universal TA.

Note 3

** indicates that a single-step rate adaptation technique is employed for these rates (see 5.5).

Note 4

Normally the user rate is derived from the network clock, and thus will reflect its stability. When network-independent clocking is used, the user data rate may differ from the nominal value by up to 100 ppm.

Note 5

It is required that the same nominal synchronous rates be used in either direction.

Data rate bit/s	Rate tolerance in %	Number of data bits	Number of stop bits	RA0/RA1 rate bit/s	RA1/RA2 rate kbit/s
50	± 2,5	5	1,5	600	8
75	± 2,5	5, 7 or 8	1; 1,5; 2	600	8
110	± 2,5	7 or 8	1 or 2	600	8
150	± 2,5	7 or 8	1 or 2	600	8
200	± 2,5	7 or 8	1 or 2	600	8
300*	± 2,5	7 or 8	1 or 2	600	8
600*	+1 -2,5	7 or 8	1 or 2	600	8
1200*	+1 -2,5	7 or 8	1 or 2	1200	8
2400*	+1 -2,5	7 or 8	1 or 2	2400	8
3600	+1 -2,5	7 or 8	1 or 2	4800	8
4800*	+1 -2,5	7 or 8	1 or 2	4800	8
7200	+1 -2,5	7 or 8	1 or 2	9600	16
9600*	+1 -2,5	7 or 8	1 or 2	9600	16
12000	+1 -2,5	7 or 8	1 or 2	19200	32
14400	+1 -2,5	7 or 8	1 or 2	19200	32
19200*	+1 -2,5	7 or 8	1 or 2	19200	32

Table 2 - Asynchronous User Rates

Note 6

* implies mandatory support by a Universal TA.

Note 7

Where split speeds are used, the RA0 and RA1 intermediate rates in both directions will be those of the highest speed.

Note 8

Where flow control is used the RA0 and RA1 intermediate rates selected may be increased.

Note 9

Number of data bits includes possible parity bits.

5.2 Asynchronous-to-Synchronous Conversion (RA0)

The RA0 function is only used with asynchronous V.-Series interfaces. Incoming asynchronous data is padded by the addition of stop elements to fit the nearest channel defined by 2^n times 600 bit/s. Thus a 300 bit/s user data signalling rate shall be adapted to a synchronous 600 bit/s stream, and a 3600 bit/s user data signalling rate to 4800 bit/s synchronous. The resultant synchronous stream is fed to RA1.

Padding with Stop elements is inhibited during the transmission of the Break signal as described in 5.2.1.

5.2.1 Break Signal

The terminal adaptor shall detect and transmit the Break signal in the following fashion.

If the converter detects m to 2m+3 bits, all of Start polarity, where m is the number of bits per character in

the selected format including Start and Stop bits, the converter shall transmit 2m+3 bits of Start polarity.

If the converter detects more than 2m+3 bits all of Start polarity, the converter shall transmit all these bits as Start polarity.

For the cases where the asynchronous rate is lower than the synchronous rate for the converter, the following rules shall apply.

The converter shall transmit Start polarity (to RA1) for a time period equal to 2m+3 bits at the asynchronous rate if the converter has detected m to 2m+3 bits of Start polarity.

If the converter has detected more than 2m+3 bits of Start polarity, the converter shall transmit (to RA1) Start polarity for an equally long time period as the received Break condition.

The 2m+3 or more bits of Start polarity received from the transmitting side shall be output to the receiving terminal.

The terminal must transmit on Circuit 103 at least 2m bits of Stop polarity after the Start polarity break signal before sending further data characters. The converter shall then regain character synchronism from the following Stop to Start transition.

5.2.2 Overspeed/Underspeed

A terminal adaptor shall insert additional Stop elements when its associated terminal is transmitting with a lower than nominal character rate. If the terminal is transmitting characters with an overspeed of up to 1% (or 2,5% in the case of nominal speeds lower than 600 bit/s), the asynchronous-to-synchronous converter may delete Stop elements as often as is necessary to a maximum of one for every eight characters at 1% overspeed. The converter on the receiving side shall detect the deleted Stop elements and reinsert them in the received data stream (Circuit 104).

The nominal length of the Start and Data elements shall be the same for all characters. The length of the Stop element may be reduced by as much as 12,5% for nominal speeds exceeding 300 bit/s to allow for overspeed in the transmitting terminal. For nominal speeds less than, or equal to, 300 bit/s a 25% reduction in Stop element is allowed.

5.2.3 Parity Bits

Possible parity bits included in the user data are considered as data bits by the RA0 function.

5.3 Adaptation to Intermediate Rates (RA1)

The RA1 function will take either the output of RA0 or the output of a synchronous V.-Series interface, and performs a bit repetition and framing function to fill an intermediate data channel of 8, 16 or 32 kbit/s.

5.3.1 Bit Repetition

A user bit repetition factor of 1, 2, 4 or 8 will be used as appropriate to rate adapt to an intermediate data channel. Bit assignment is specified in 5.3.2.5.

5.3.2 Frame Structure

An 80-bit frame is used, as shown in Table 3.

The octet zero contains eight ZEROs, whilst octet five consists of a ONE followed by seven E-bits. In octets one to four, and six to nine, bit one is set to ONE, bit eight is a status bit (S or X) and bits two to seven are data bits (D). The order of transmission is from left to right and top to bottom.

Octet Number	Bit Number							
	one	two	three	four	five	six	seven	eight
zero	0	0	0	0	0	0	0	0
one	1	D1	D2	D3	D4	D5	D6	S1
two	1	D7	D8	D9	D10	D11	D12	X
three	1	D13	D14	D15	D16	D17	D18	S3
four	1	D19	D20	D21	D22	D23	D24	S4
five	1	E1	E2	E3	E4	E5	E6	E7
six	1	D25	D26	D27	D28	D29	D30	S6
seven	1	D31	D32	D33	D34	D35	D36	X
eight	1	D37	D38	D39	D40	D41	D42	S8
nine	1	D43	D44	D45	D46	D47	D48	S9

Table 3 - Frame Structure

5.3.2.1 Frame Synchronization Bits

The 17-bit frame alignment pattern consists of all eight bits of octet zero (set to ZERO), and all bits in position one (set to ONE) of the following nine octets.

5.3.2.2 S and X Bits

Bits S and X are used to convey channel control information associated with the data bits in the data transfer state, as shown in Table 4. The S-bits are put into two groups SA and SB, to carry the condition of two interchange circuits. The X-bit is used to carry the condition of Circuit 106, and in addition, signals the state of frame synchronization between TAs. The X-bit can also be used optionally to carry flow control information between TAs supporting asynchronous terminal equipment, in which case direct control of Circuit 106 may not be required and may be disabled. This usage is specified in Clause 9.

The use of S- and X-bits for synchronization of entry to, and exit from, the data transfer phase is specified in Clause 7.

108	S1, S3, S6, S8 (= SA)	107
105	S4, S9 (= SB)	109
Frame sync. Flow Control	X	106

Table 4 - Interchange Mapping Scheme

Note 10

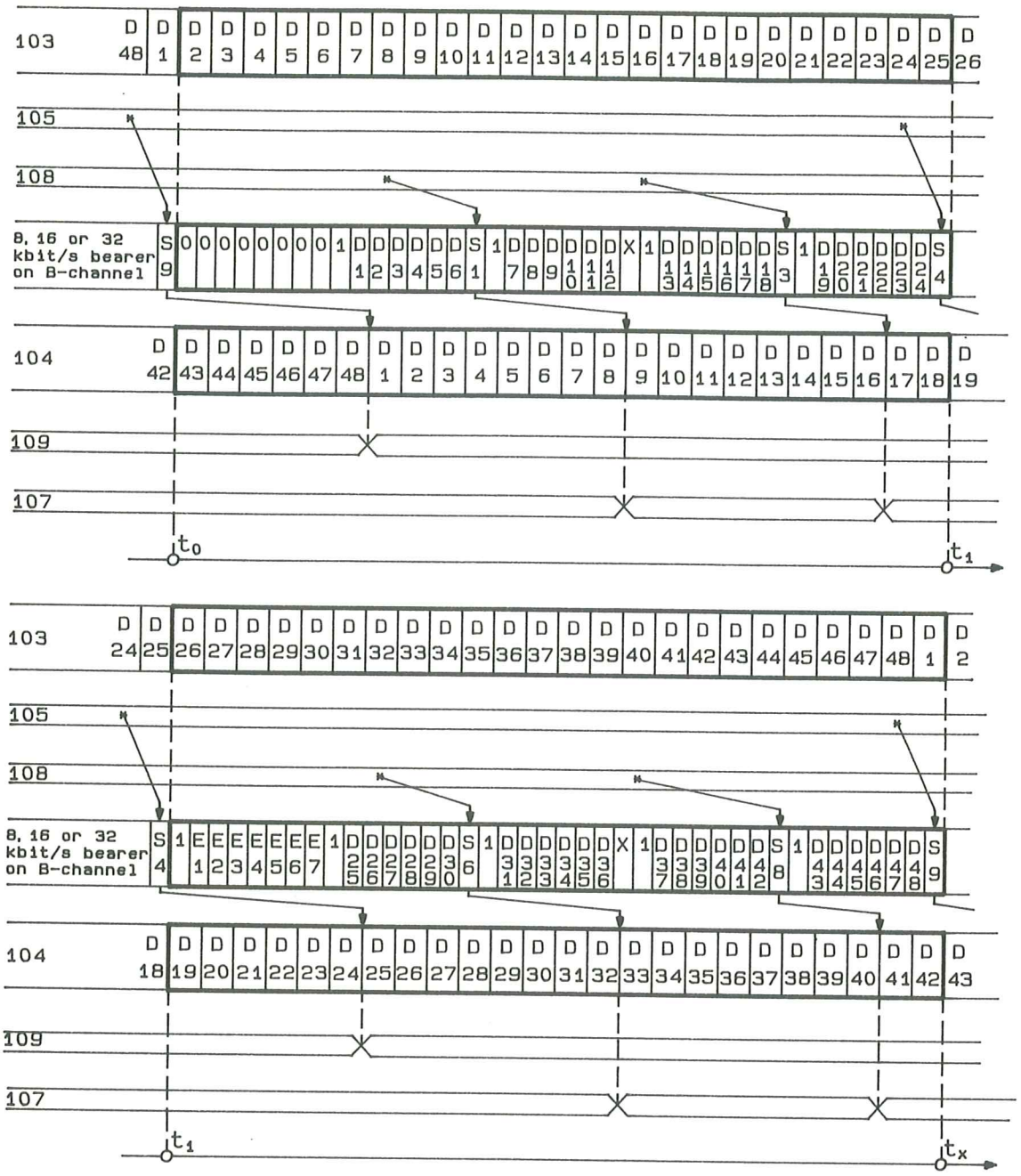
For the S- and X-bits, a ZERO corresponds to the ON condition, a ONE to the OFF condition.

Control information conveyed by the S-bits, and user data conveyed by the D-bits, should not have different transmission delays. The S-bits should therefore transmit control information sampled simultaneously with the D-bits in the positions specified in Table 5, and as presented in Figure 4.

The X-bit shall be presented upon arrival to control Circuit 106 which shall respond as defined in 6.3, or shall perform a flow control procedure as described in Clause 9.

S-Bit	Octet No.	Bit No.
S1	2	3 (D8)
S3	3	5 (D16)
S4	4	7 (D24)
S6	7	3 (D32)
S8	8	5 (D40)
S9	9	7 (D48)

Table 5 - Coordination of S-bits to D-bits



* indicates the sampling point for Circuit 105 and 108
X indicates the change point for Circuits 107 and 109

Figure 4 - Coordination of S-bits to D-bits

5.3.2.3 E-bits

The E-bits are used to carry following information:

- Bit repetition identification (E1, E2, E3).

They may also be used to carry:

- Network independent clock information (E4, E5, E6),
- Multi-frame synchronization (E7).

The coding of the E-bits is shown in Table 6.

Intermediate Rates kbit/s			E-bits						
8	16	32	E1	E2	E3	E4	E5	E6	E7
bit/s	bit/s	bit/s							
600			1	0	0	C	C	C	M
1200			0	1	0	C	C	C	1
2400			1	1	0	C	C	C	1
	7200	14400	1	0	1	C	C	C	1
4800	9600	19200	0	1	1	C	C	C	1

Table 6 - E-bit usage

Note 11

M: In order to maintain compatibility with CCITT Rec. I.461, for the 600 bit/s user rate E7 is coded so as to enable multi-frame synchronization. E7 in the fourth 80-bit frame is set to ZERO. See Table 7A.

Note 12

C indicates the use of E4, E5 and E6 for the transport of network-independent clocking information. These bits are set to ONE when unused.

Note 13

Asynchronous rate information must be determined by the use of out-of-band signalling. Synchronous rate inform-ation may be determined by use of E1, E2 and E3 in conjunction with the intermediate rate.

5.3.2.4 D-Bits

Data are conveyed in D-bits, i.e. up to 48 such bits per 80-bit frame. In this Standard the octet boundaries of the user's data stream are not defined.

5.3.2.5 Bit Assignment

The adaptation of the 600, 1200 and 2400 bit/s rates to the 8 kbit/s intermediate rate including user bit repetition are shown in Tables 7A, 7B and 7C respectively. The adaptation of 7200 and 14400 bit/s rates to the 16 and 32 kbit/s intermediate rates respectively, use the data bit assignments shown in Table 7D. The adaptation of 4800, 9600 and 19200 bit/s to the 8, 16 and 32 kbit/s intermediate rates respectively, use the data bit assignments shown in Table 7E.

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D1	D1	S1
1	D1	D1	D2	D2	D2	D2	X
1	D2	D2	D2	D2	D3	D3	S3
1	D3	D3	D3	D3	D3	D3	S4
1	1	0	0	E4	E5	E6	M
1	D4	D4	D4	D4	D4	D4	S6
1	D4	D4	D5	D5	D5	D5	X
1	D5	D5	D5	D5	D6	D6	S8
1	D6	D6	D6	D6	D6	D6	S9

Table 7A

0	0	0	0	0	0	0	0
1	D1	D1	D1	D1	D2	D2	S1
1	D2	D2	D3	D3	D3	D3	X
1	D4	D4	D4	D4	D5	D5	S3
1	D5	D5	D6	D6	D6	D6	S4
1	0	1	0	E4	E5	E6	1
1	D7	D7	D7	D7	D8	D8	S6
1	D8	D8	D9	D9	D9	D9	X
1	D10	D10	D10	D10	D11	D11	S8
1	D11	D11	D12	D12	D12	D12	S9

Table 7B

0	0	0	0	0	0	0	0
1	D1	D1	D2	D2	D3	D3	S1
1	D4	D4	D5	D5	D6	D6	X
1	D7	D7	D8	D8	D9	D9	S3
1	D10	D10	D11	D11	D12	D12	S4
1	1	1	0	E4	E5	E6	1
1	D13	D13	D14	D14	D15	D15	S6
1	D16	D16	D17	D17	D18	D18	X
1	D19	D19	D20	D20	D21	D21	S8
1	D22	D22	D23	D23	D24	D24	S9

Table 7C

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	F	F	X
1	D11	D12	F	F	D13	D14	S3
1	F	F	D15	D16	D17	D18	S4
1	1	0	1	E4	E5	E6	1
1	D19	D20	D21	D22	D23	D24	S6
1	D25	D26	D27	D28	F	F	X
1	D29	D30	F	F	D31	D32	S8
1	F	F	D33	D34	D35	D36	S9

Table 7D

0	0	0	0	0	0	0	0
1	D1	D2	D3	D4	D5	D6	S1
1	D7	D8	D9	D10	D11	D12	X
1	D13	D14	D15	D16	D17	D18	S3
1	D19	D20	D21	D22	D23	D24	S4
1	0	1	1	E4	E5	E6	1
1	D25	D26	D27	D28	D29	D30	S6
1	D31	D32	D33	D34	D35	D36	X
1	D37	D38	D39	D40	D41	D42	S8
1	D43	D44	D45	D46	D47	D48	S9

Table 7E

Table 7A: Adaptation of 600 bit/s synchronous rate to 8 kbit/s intermediate rate. M: see Note 11.

Table 7B: Adaptation of 1200 bit/s synchronous rate to 8 kbit/s intermediate rate.

Table 7C: Adaptations of 2400 bit/s synchronous rate to 8 kbit/s intermediate rate.

Table 7D: Adaptation of n x 3600 bit/s synchronous rate to the appropriate intermediate rate, n is 2 or 4 only.

Table 7E: Adaptation of n x 4800 bit/s synchronous rate to the intermediate rate, n is 1, 2 or 4 only.

5.3.3 Frame Synchronization Procedure

The following 17-bit alignment pattern in the 80-bit frame is used to achieve frame synchronization:

00000000 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX
1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX 1XXXXXXX

It is assumed that the error rate will be sufficiently low to expect frame synchronization following the detection of one 80-bit frame.

5.3.3.1 Frame Synchronization Monitoring and Recovery

The monitoring of the frame synchronization shall be a continuous process using the same procedures as for initial detection.

Loss of frame synchronization shall not be assumed unless at least three consecutive frames, each with at least one framing bit error, are detected. Procedures following loss of frame synchronization are specified in 7.1.5.

5.4 Adaptation of Intermediate Rates to 64 kbit/s (RA2)

Since the rate adaptation of a single intermediate rate (either 8, 16, or 32 kbit/s generated by the RA1 function) to the 64 kbit/s B-channel rate must be compatible to enable interworking, a common approach is needed for the second step rate adaptation, and possibly for intermediate rate multiplexing. This second step rate adaptation method is specified in CCITT Rec. I.460.

Note 14

Orientation of the 80-bit frame within the 16 or 32 kbit/s channel is not assumed.

5.5 Adaptation of 48 and 56 kbit/s User Rates to 64 kbit/s

The 48 and 56 kbit/s user data rates are adapted to 64 kbit/s B-channel rate in one step as indicated in Tables 8 and 9 respectively. It is required that the octets of the frames shown in these Tables be aligned with the PCSN octet timing.

Octet Number	Bit Number							
	one	two	three	four	five	six	seven	eight
one	1	D1	D2	D3	D4	D5	D6	S1
two	0	D7	D8	D9	D10	D11	D12	X
three	1	D13	D14	D15	D16	D17	D18	S3
four	1	D19	D20	D21	D22	D23	D24	S4

Table 8 - Adaptation of 48 kbit/s user rate to 64 kbit/s

Note 15

See 5.3.2.2 for the use of bits S1, S3, S4 and bit X. However, for international interworking purposes, bit X must be set to ONE.

Note 16

Network-independent clocking cannot be supported in this case.

Note 17

Octet orientation of the 32-bit frame within the 64 kbit/s channel is required.

Octet Number	Bit Number							
	one	two	three	four	five	six	seven	eight
one	D1	D2	D3	D4	D5	D6	D7	1
two	D8	D9	D10	D11	D12	D13	D14	1
three	D15	D16	D17	D18	D19	D20	D21	1
four	D22	D23	D24	D25	D26	D27	D28	1
five	D29	D30	D31	D32	D33	D34	D35	1
six	D36	D37	D38	D39	D40	D41	D42	1
seven	D43	D44	D45	D46	D47	D48	D49	1
eight	D50	D51	D52	D53	D54	D55	D56	1

Table 9 - Adaptation of 56 kbit/s user rate to 64 kbit/s

Note 18

Octet orientation of the 64-bit frame within the 64 kbit/s channel is required.

Note 19

Neither network-independent clocking nor interchange circuits can be supported in this case.

6. INTERCHANGE CIRCUITS

6.1 List of Interchange Circuits

The interchange circuits which may be of interest in this Standard are listed in Table 10.

All interchange circuits which are provided shall comply with the functional and operational requirements of CCITT Rec. V.24.

6.2 Timing Arrangements

The TA shall derive its timing from the received bit stream of the TA/network interface. This timing will be used by the TA to provide the connected synchronous equipment with transmitter element timing on Circuit 114 and receiver element timing on Circuit 115. However, for cases where the equipment is unable to accept timing (e.g. a synchronous modem), it will be necessary to carry clocking information across the link. A method is defined in Clause 8. A TA implementing this option will generate and utilize clocks which are thus not necessarily synchronized to the network.

Circuit	Interchange Description	Notes
103	Transmitted data	
104	Received data	
105	Request to send	Note 20
106	Ready for sending	
107	Data set ready	
108.1 or 108.2	Connect data set to line	Note 21
109	Data terminal ready	Note 21
	Data channel received line signal detector	
111	Data signalling rate selector (DTE)	Note 22
112	Data signalling rate selector (DCE)	Note 22
113	Transmitter signal element timing (DTE)	Note 23
114	Transmitter signal element timing (DCE)	
115	Receiver signal element timing (DCE)	
125	Calling indicator	Note 24
140	Loopback/maintenance test	Note 25
141	Local loopback	Note 25
142	Test indicator	Note 25

Table 10 - Interchange Circuits

Note 20

Not required for DTEs that operate with DCEs in the «continuous carrier mode».

Note 21

This circuit shall be capable of operation as Circuit 108.1 or Circuit 108.2 depending on its use.

Note 22

The use of this circuit is outside the scope of this Standard.

Note 23

The use of Circuit 113 requires the support of network-independent clocking, as described in Clause 8.

Note 24

This circuit is used with the automatic answering terminal adaptor function.

Note 25

The use of loopback testing is outside the scope of this Standard.

6.3 Circuit 106

After the start-up and synchronization recovery sequences, the ON state of Circuit 106 shall be delayed relative to the ON state of Circuit 105 (where implemented, provided that the X-bit is ON) by an interval of at least 24 user data bits. ON to OFF transitions of Circuit 106 shall follow ON to OFF transitions of Circuit 105 (when implemented) by less than 2 ms. Where Circuit 105 is not implemented the initial Circuit 106 transition to the ON state shall be delayed by at least 24 user data bits relative to the corresponding transitions in the state of Circuit 109. Subsequent transitions in the state of Circuit 106 should occur solely in accordance with the operating sequences defined in Clause 7.

6.4 Circuit 109

OFF to ON and ON to OFF transitions of Circuit 109 should occur solely in accordance with the operating sequences defined in Clause 7.

7. OPERATING SEQUENCES

7.1 TA Duplex Operation

When using a TA to provide alternate voice/data service within a PCSN, the call is established in the (end-to-end) digital mode using the procedures applicable to the particular network (or networks) and/or terminal configuration. Voice coordination is used to determine compatibility issues such as: data signalling rate, duplex vs. half-duplex, etc.

It is assumed that some internal means is provided for the TE-1 to control the transfer from the voice to the data mode and from the data to the voice mode. For information purposes, some of the duplex operational sequences are also shown in Figure 5. This figure shows only an example of a successful call procedure.

7.1.1 Idle (or Ready) State

During the idle (or ready) state the TA (DCE) will receive the following from the DPE:

Circuit 103 = continuous ONEs,
Circuit 105 = *,
Circuit 108.1 = OFF or Circuit 108.2 = ON.

* In many duplex DPEs Circuit 105 is either permanently in the ON condition or is not present. If not present, the function must be set to an ON condition in the TA. See 7.1.2 for the case where a duplex DPE can operate Circuit 105.

During the idle (or ready) state the TA will transmit continuous ONEs into the B-channel (i.e. all data, framing and status bits set to ONE).

During the idle (or ready) state the TA (DCE) will transmit the following toward the DPE:

Circuit 104 = continuous ONEs,
Circuit 107 = OFF,
Circuit 106 = OFF,
Circuit 109 = OFF.

7.1.2 Connect TA to Line State

Upon transition from the voice to the data mode, Circuit 108, if not previously ON, is switched from the OFF to the ON condition.

Note 26

The manual transfer from voice to data must occur at approximately the same time at both ends of the connection.

Switching to the data mode causes the TA to transmit the following toward the network (refer to Table 3: Frame Structure):

i) Frame synchronization pattern, as follows:

Octet zero = all ZEROs, bit one of octets one to nine set to ONE,

ii) Data bits = ONE,

iii) Status bits S = OFF and X = OFF.

Note 27

At this time Circuit 103 is not connected to the «data channel» (e.g. the condition of the data bits is generated within the TA).

At this time (i.e. switching to data mode) the receiver in the TA will begin to search for the frame synchronization pattern in the received bit stream (see 5.3.2).

At the same time, the timer T1 (see Figure 5) shall be started with a time-out value of at least 10 seconds.

When the receiver recognizes the frame synchronization pattern it causes the S- and X-bits in the transmitted frames to be turned ON.

When the receiver recognizes that the status bits S and X are in the ON condition it will perform the following functions:

i) Turn ON Circuit 107 toward the DPE and stop timer T1;

Note 28

A duplex DPE that implements and is able to operate Circuit 105 may be expected to turn this Circuit ON at any time. However, if not previously turned ON, it must be turned ON in response to the ON condition on Circuit 107.

ii) At this time Circuit 103 may be connected to the «data bits» in the frame; however, the DPE must maintain a ONE condition until Circuit 106 is turned ON in the next portion of the sequence;

iii) Turn ON Circuit 109 and connect the «data bits» to Circuit 104;

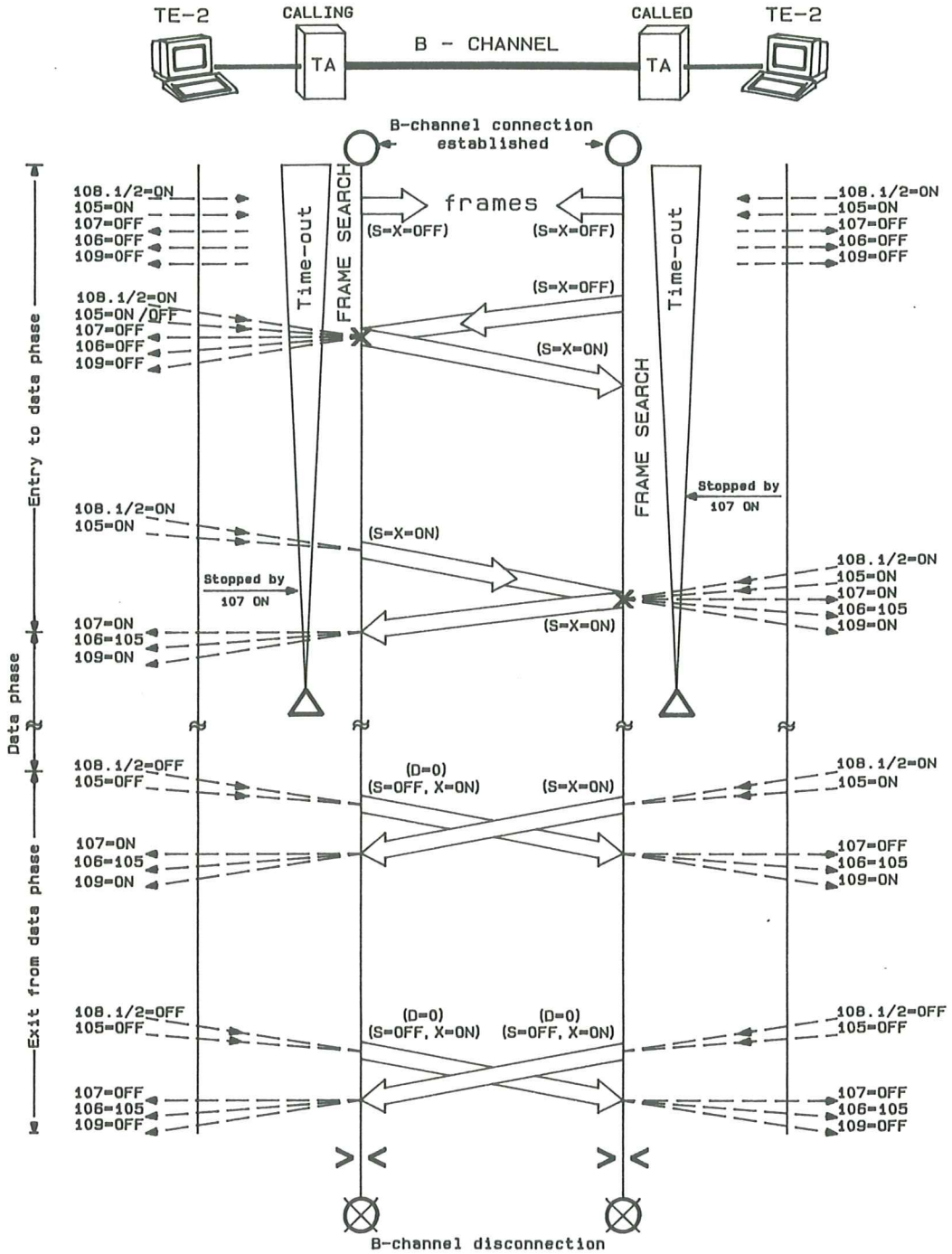
Note 29

ONE is being received on Circuit 104, at this time.

iv) After an interval of at least 24 bits of user data, it will turn ON Circuit 106.

v) A transition in Circuit 106 from OFF to ON will cause a transition in Circuit 103 from ONE to the «data mode».

If Circuit 107 has not been turned ON after expiry of timer T1, the terminal adaptor shall be disconnected according to the procedures given in 7.1.4.



○ B-channel connection of TA

⊗ B-channel disconnection of TA

× Bidirectional switch-through TE2

>< Bidirectional disconnection of TE2

△ TA disconnecting procedure according to 7.1.4 started

Figure 5 - TA Synchronization of entry to and exit from data transfer phase

7.1.3 Data Transfer State

Whilst in the data transfer state the following circuit conditions exist:

i) Circuits 105 (when implemented), 106, 107, 108.1 or 108.2 and 109 are in the ON condition,

ii) Data are being transmitted on Circuit 103 and received on Circuit 104.

7.1.4 Disconnect or Return to Voice Mode

At the completion of the data transfer phase, the local DPE will indicate a «Disconnect Request» by turning OFF Circuit 108. This will cause the following to occur:

i) The Status bits S in the outgoing frame will be set to OFF, Status bits X are kept ON,

ii) Circuit 106 will be turned OFF,

iii) The data bits in the frame will change from «data» to ZERO.

If Circuit 108 is still ON at the remote TA, this TA will recognize the transition of the status bits from ON to OFF and the data bits from «data» to ZERO as a disconnect signal and it will turn OFF Circuits 107 and 109. This DPE should respond by turning OFF Circuit 108 and transferring to the «Voice Mode». If the TE-1 is «Off-hook» the connection will be maintained in the voice mode. If the TE-1 is «On-hook» the TE-1 will control the disconnection via signalling. At this time, the TA will return to the idle (or ready) state.

The TA at the station that originated the disconnect request will recognize the reception of S = OFF or loss of framing signals as a «Disconnect Acknowledgement» and turn OFF Circuits 107 and 109 and transfer to the voice mode. If the TE-1 is «Off-hook» the connection will be maintained in the voice-mode. If the TE-1 is «On-hook», the TE-1 will control the disconnection via the signalling. At this time the TA will return to the idle (or ready) state.

7.1.5 Loss of Frame Synchronization

In the event of loss of frame synchronization on the B-channel the TA should attempt to resynchronize as follows:

i) Set Circuit 104 from «Received Data» to continuous ONEs.

ii) Turn OFF status bit X in the transmitted frame.

iii) The remote TA upon recognition of status bit X OFF will turn OFF Circuit 106 which will cause the DPE to place Circuit 103 in a continuous ONEs condition.

Note 30

The use of a flow control protocol as specified in Clause 9 may cause a modification of this action.

iv) The local TA should attempt to resynchronize on the incoming signal.

v) If after an interval of 3 seconds it cannot attain synchronization, it should send a «disconnect request» by turning OFF all of the status bits for three frames with data bits set to ZERO and then disconnecting by turning OFF Circuit 107 and transferring to the voice mode as discussed in 7.1.4 above.

vi) If synchronization is achieved, the TA should turn ON status bit X towards the distant station.

vii) Upon recognition of Status bit set to ON, the remote TA will turn ON Circuit 106, allowing the DPE to recommence transmission of data on Circuit 103.

Note 31

The use of a local flow control protocol as specified in Clause 9 may cause a modification of this action.

Note 32

During a resynchronization attempt, Circuits 107 and 109 will remain ON.

7.2 TA-A Half-Duplex Operation

The alternate voice/data call establishment and voice coordination for the interworking of half-duplex DPEs equipped with V.-Series type interfaces is the same as discussed in 7.1. The only difference between half-duplex and duplex operation is in the control of the Circuits 105, 106 and 109, as follows:

Note 33

A half-duplex DPE may not be able to interwork with a V.-Series or an X.-Series duplex DPE (TE-2).

In a TA arranged to accommodate half-duplex DPEs, Circuit 109 will be under the control of the status bits SB in the incoming frame, as follows:

i) If at the local interface Circuit 109 is OFF and Circuit 104 is in the ONE state, the DPE may «Request to send» by turning ON Circuit 105.

ii) The TA will then turn ON Status bits SB in the transmitted frame which will turn ON Circuit 109 in the remote interface and connect Circuit 104 to the data bit stream of the incoming frame.

iii) After an interval of at least 24 user data bits (see 6.3) the local TA will turn ON Circuit 106, which will allow the local DPE to transmit data on Circuit 103.

iv) Upon completion of the transmission the local DPE will turn OFF Circuit 105. This will then:

- Turn OFF Circuit 106 in the local interface and Circuit 103 will revert to the continuous ONEs state.
- Turn OFF status bits SB which will turn OFF Circuit 109 and place Circuit 104 in a ONE condition at the remote TA.

v) At this time the remote DPE is able to reverse the sequence by turning ON Circuit 105.

7.3 TA-B

The mapping of V.25 and/or V.25bis automatic calling and/or automatic answering procedures to the network signalling protocols is outside the scope of this Standard.

8. NETWORK-INDEPENDENT CLOCKS

In cases where synchronous data signals at user rates up to and including 19,2 kbit/s are received from outside the digital PCSN which are not synchronized to the PCSN timing, the following method shall be used to enable transfer of those data signals and the corresponding bit timing information via the 80-bit frame to a receiving TA. Such a case will apply when signals are received by an interworking unit from voice-band data modems in the analogue PSTN. The frequency tolerance of such modems is within the limits of $\pm 10^{-4}$ relative to the nominal data rate.

This clause defines:

i) The rules for measuring phase differences between PCSN timing and the received modem bit timing,

ii) The compensation procedure,

iii) The coding of the corresponding information into the 80-bit frame.

8.1 Measurement of Phase Differences

The phase difference between the following two frequences will be measured:

i) R1 = 0,6 x the nominal intermediate rate (except where Fill bits are used; see Note 34), synchronized with the digital PCSN,

ii) R2 = 0,6 x the nominal intermediate rate (except where Fill bits are used; see Note 34), derived from and synchronized with the bit timing received from the synchronous voice-band modem.

Note 34

Clocks R1 and R2 are nominally either 4800, 9600 or 19200 Hz at 8 kbit/s, 16 kbit/s and 32 kbit/s intermediate rates respectively.

Where Fill bits are used, in the cases of 7200 bit/s and 14400 bit/s, R1 and R2 will have the same nominal rate as the user bit rate.

Compensation will affect one, one-half, one-quarter or one-eighth of a user data bit, dependent upon the bit repetition factor.

A state diagram for the transmitting TA showing the phase of R2 relative to R1 appears in Figure 6. Table 11 shows the related bit coding.

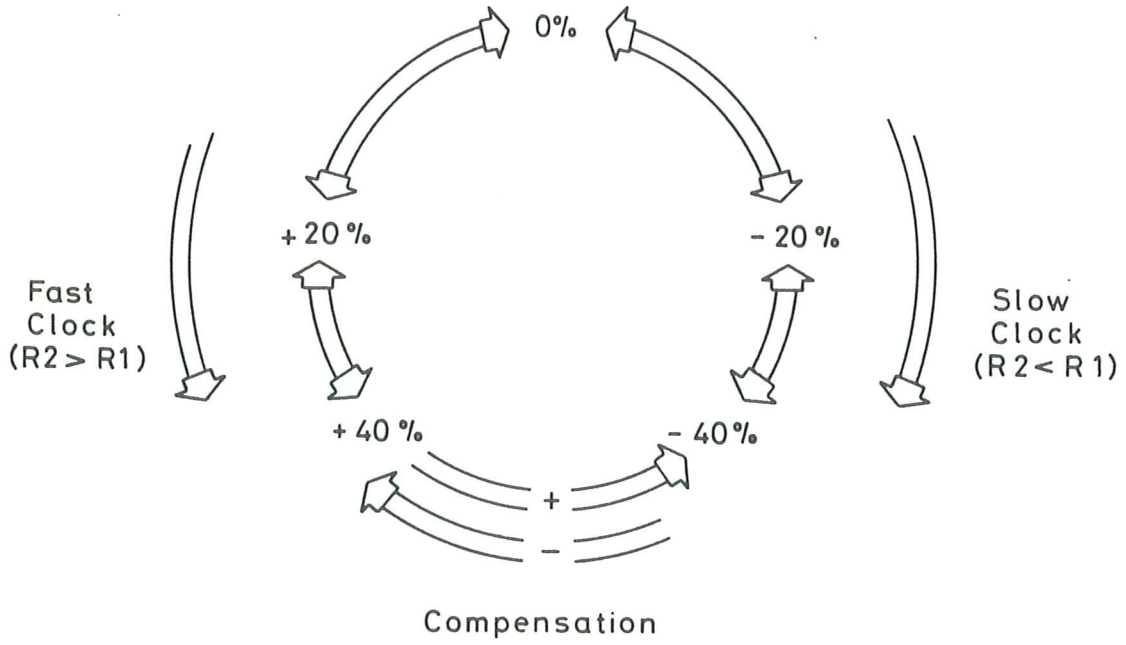


Figure 6 - Network-Independent Clocking State Diagram

Note 35

Phase measurements are given relative to R1 by the formula below:

Phase = phase(R2) - phase(R1)

Note 36

Receipt of a bit combination requiring an illegal move of more than one state will cause a legal move of one state in the appropriate direction.

Note 37

The initial state for both the receiving and transmitting sides of the TA will be 0%.

Comparison of R1 and R2 will give a phase difference relative to R1 which will be encoded as shown in Table 11. The resultant 3-bit code will be transmitted in bit positions E4, E5 and E6, and used for clock control at the receiving TA.

To avoid continuous jitter between neighbouring displacement positions, hysteresis shall be applied, as follows:

The displacement code shall be changed only when the measured phase difference between R1 and R2 is 15% (of the R1 clock period) more or less than the difference indicated by the existing displacement code.

Example: Bit combination 000 indicates a phase difference of nominally 20%. This bit combination will be changed into 001 when the measured phase difference is 35% or more, and into 111 when the measured phase difference is 5% or less.

8.2 Positive/Negative Compensation

On transition from the +40% state to the -40% state an extra user D bit has to be transmitted in the 80-bit frame, using bit E6 (positive compensation). At the receiving TA this extra bit will be inserted between D24 and D25 as shown in Table 3, immediately following the E-bits.

On transition from the -40% state to +40% state a bit combination is transmitted in the 80-bit frame (E4, E5, E6 = 1, 1, 0 respectively), indicating to the receiving TA that bit D25 of the 80-bit frame, being set to ONE, does not contain user data and should be removed (negative compensation).

8.3 Encoding

The encoding of the measured phase difference for clock control and the positive/negative compensation control overrides and replaces the clock control coding.

Displacement (in % of nominal R1 clock period at n x 4800 bit/s, n=1, 2 or 4)		Coding in the 80-bit frame		
		E4	E5	E6
nominally	0	1	1	1
	+ 20	0	0	0
	+ 40	0	0	1
	- 40	0	1	0
	- 20	0	1	1
Compensation control		E4	E5	E6
Positive compensation of a one		1	0	1
Positive compensation of a zero		1	0	0
Negative compensation		1	1	0

Table 11 - Coding of E-bits for Network-Independent Clocking

9. FLOW CONTROL

This Clause describes an option which may be used between TAs supporting asynchronous terminals. Flow control allows the connection of asynchronous terminals operating at different user data rates by reducing the character output of the faster to that of the slower. Support of flow control will require the use of the defined end-to-end protocol and an incoming line buffer in addition to a selected local protocol. Depending upon the local flow control protocol employed, there will also be a requirement for character buffering from the terminal interface. The size of this buffer is not determined in this Standard, as it is dependent upon implementation.

9.1 Local Flow Control: TA to DPE

Connection may be made between TAs connected to asynchronous terminal equipment operating at two different speeds. It is the responsibility of the TA connected to the faster DPE to execute a local flow control protocol to reduce the character

rate to that of the slower DPE. This operation will require some buffer storage in the TA. A TA may support several different local flow control protocols, although only one will be selected at any time. There are a number of such protocols in use, some of which are detailed in the following text.

9.1.1 105/106 Operation

This is an out-of-band flow control mechanism, utilizing two of the interchange Circuits of the V.-Series interface. If a DPE requires to transmit a character, it turns ON Circuit 105 (Request to Send). The DPE can only begin transmission when it receives in return Circuit 106 ON (Ready for Sending). If, during transmission of a block of characters Circuit 106 goes OFF, the DPE must cease transmission until Circuit 106 turns ON again.

9.1.2 XON/XOFF Operation

This is an in-band flow control mechanism using two characters of the IA5 set for XON and XOFF operation. If a DPE receives an XOFF character it must cease transmission. When the DPE receives an XON character it may resume transmission. The characters typically used for XON and XOFF are DC1 and DC3 (bit combination 1/1 and 1/3 in Standard ECMA-6) respectively, although alternative bit combinations can be used.

9.1.3 Other Methods

Alternative and non-standardized methods of asynchronous flow control are in use, and these may be mapped onto the TA flow control protocol.

9.2 End-to-End Flow Control: TA to TA

Reduction of the character rate is not sufficient to guarantee correct operation, and end-to-end flow control is used.

The X-bit is used to carry flow control information. A TA will buffer incoming characters. When the number of buffered characters exceeds a threshold TH1, dependent upon implementation, the TA will set the X-bit of its outgoing frames to OFF.

Upon receipt of a frame containing an X-bit set to OFF, a TA will execute its selected local flow control procedure indicating that the attached DPE must stop sending characters, and cease the transmission of data after completion of the character in progress by setting the data bits in outgoing frames to ONE.

When the buffer contents of a TA which has initiated an end-to-end flow control drops below threshold TH2, the TA will reset the outgoing X-bit to ON.

When the far-end TA receives a frame with X-bit set to ON, it will recommence data transmission, and by use of the local flow control procedure indicate to the attached DPE that it may continue sending characters.

Note 38

There will be a delay between initiation of the end-to-end flow control protocol and termination of the incoming character stream. The characters arriving during this time must be

buffered, and the total buffer size will depend upon the character rate, round-trip delay and the buffer threshold TH1.

9.3 Use of Channel Capacity

Upon accepting a call from a TA supporting flow control and operating at a different user rate and/or intermediate rate, the called TA will adopt the identical intermediate rate and bit repetition factor. This will override the parameters normally selected. In such cases the TA connected to the faster DPE will execute a local flow control procedure to reduce the character rate to that of the slower DPE.

Thus if a faster DPE calls a slower DPE, the faster intermediate channel rate and bit repetition factor will be adopted at both ends, and the calling TA will utilize local flow control. If a slower DPE calls a faster DPE, the slower intermediate channel rate and bit repetition factor will be adopted, and the called TA will utilize local flow control.

9.4 Requirements of a TA supporting Flow Control

The following are general requirements for a TA supporting flow control:

i) A TA supporting flow control shall be capable of operating with an intermediate rate and bit repetition factor that is independent of the asynchronous speed used at its terminal interface.

ii) A TA supporting flow control shall be capable of recognizing the intermediate rate and bit repetition factor required for an incoming call, and adopting it. User rate information will be obtained from signalling.

iii) A TA supporting flow control shall be capable of executing a local flow control protocol to reduce the character rate to that of the far-end DPE.

iv) A TA supporting flow control will support the use of end-to-end flow control using the X-bit, and will contain a character buffer.

10. INTERWORKING

10.1 General Interworking Cases

Interworking with DPEs which have interfaces that conform with one of the following CCITT Recommendations is considered.

i) X.21, user classes of service 3 to 7 defined in CCITT Rec. X.1,

ii) X.21bis, user classes of service 3 to 7 defined in CCITT Rec. X.1,

iii) V.-Series, using data rates defined in CCITT Recs. V.5 or V.6,

iv) V.-Series, with data rates defined in Table 2 for asynchronous use.

Interworking cases which may be supported by a terminal adaptor are listed in the following sub-clauses. Included is interworking of DPEs with different interface types connected

to the same PCSN, and interworking between a DPE on a PCSN and a DPE on another network.

Inter-network synchronization is required for cases (i) and (ii). If network-independent clocking is used network synchronization is not required for cases (iii) and (iv).

10.2 Synchronous DPEs with V.-Series Interfaces (including X.21bis)

Table 12 shows the allowed interworking configurations.

V.-Series synchronous DPE	V.-Series synchronous DPE
on one PCSN	on same PCSN on ISDN on PSTN (IWU & modem) on another PCSN: direct via ISDN via PSTN

Table 12 - Allowed V.-Series synchronous interworking cases

Note 39

The possible data rates may be restricted in specific config-urations due to the inherent limitation of the relevant net-works, e.g. to 9600 bit/s at present for a PSTN.

10.3 Synchronous V.-Series DPEs with X.21 DPEs

Table 13 shows the allowed interworking configurations for X.21 DPEs conforming to user classes of service 3 to 7 of CCITT Rec. X.1.

V.-Series synchronous DPE	X.21 DPE
on one PCSN	on same PCSN on ISDN on CSPDN on another PCSN: direct via ISDN via CSPDN

Table 13 - Allowed V.-Series and X.21 interworking cases

As V.-Series interfaces do not support octet orientation, interworking between a V.-Series TA and a X.30 TA is not possible in cases which require this.

10.4 Asynchronous V.-Series DPEs with Asynchronous V.-Series DPEs

Table 14 shows allowed interworking configurations.

V.-Series asynchronous DPE	V.-Series asynchronous DPE
on one PCSN	on same PCSN on ISDN on PSTN on another PCSN: direct via ISDN via PSTN

Table 14 - Allowed V.-Series asynchronous interworking cases

11. PERFORMANCE MONITORING

Only monitoring functions which are directly related with the rate adaptation scheme specified in this Standard, are considered here.

Frame synchronization, as defined in 5.3.3 must be monitored continuously. Actions to be taken if frame synchronization is lost or achieved are described in 7.1.5. Any other actions are outside the scope of this Standard.

The following parameters may be monitored:

- Total number of bit errors per call,
- Total number of erroneous seconds per call,
- Total number of times frame synchronization has been lost during the call,
- Total time of loss of frame synchronization during the call.

Bit errors and erroneous seconds are only counted when in a synchronized state as defined in 5.3.3.

The use of the above parameters is outside the scope of this Standard.

APPENDIX A

SUMMARY OF CHANGES INCORPORATED IN THE 2ND EDITION OF STANDARD ECMA-102

This Second Edition of Standard ECMA-102 clarifies and provides explanatory text for a number of details which will ease implementation of the Standard:

The BREAK signal has been enhanced to clarify handling of Break signals and Stop elements (see 5.2.1).

The use of S- and X-bits to convey channel control information in association with the data bits is limited to the data transfer state (see 5.3.2.2).

Figure 4 has been enhanced to portray the coordination of S- and D-bits in a complete 80-bit frame.

In Figure 5, the timer shown has now a specified time-out value to provide sufficient response time for non-ISDN networks, and prevents ineffective communication. Handling of this timer and actions required are described in 7.1.2.