ecma INTERNATIONAL

Standard ECMA-369

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MAC-PHY Interface for ECMA-368

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Standard

ECMA-369

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MAC-PHY Interface Specification for ECMA-368

Introduction

ECMA-368 specifies the PHY and MAC for a high rate ultra wideband wireless transceiver. Implementations of ECMA-368 may expose the interface between the PHY and MAC as specified herein.

This Ecma Standard has been adopted by the General Assembly of December 2005.

Table of contents

1 Scope

This Ecma Standard specifies the interface between implementations of the PHY and MAC as specified in ECMA-368.

2 Conformance

PHY and MAC implementations of ECMA-368 conform to this Standard by implementing the interface specified herein.

3 References

ECMA-368 High Rate Ultra Wideband PHY and MAC Standard

4 Definitions

For the purposes of this document, the definitions given in ECMA-368 apply.

5 Notational Conventions

The use of the word *shall* is meant to indicate a requirement which is mandated by the Standard, i.e. it is required to implement that particular feature with no deviation in order to conform to the Standard. The use of the word *should* is meant to recommend one particular course of action over several other possibilities, however without mentioning or excluding these others. The use of the word *may* is meant to indicate that a particular course of action is permitted. The use of the word *can* is synonymous with is able to – it is meant to indicate a capability or a possibility.

All floating-point values have been rounded to 4 decimal places.

An exclamation mark preceding a signal indicates that the signal is active low.

6 Abbreviations and Acronyms

BM	Burst Mode
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Code
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FCS	Frame Check Sequence
FFI	Fixed-Frequency Interleaving
FRC	Free Running Clock
HCS	Header Check Sequence
LQI	Link Quality Indicator
lsb	Least-Significant Bit
MAC	Medium Access Control
MBOA	Multiband OFDM Alliance
MIFS	Minimum Interframe Space

msb	Most-Significant Bit
OFDM	Orthogonal Frequency Division Modulation
PHY	Physical (layer)
PLCP	Physical Layer Convergence Protocol
PPM	Parts per Million
PT	Preamble Type
RSSI	Received Signal Strength Indicator
RX	Receive or Receiver
SIFS	Short Interframe Space
TF	Time-Frequency
TFC	Time-Frequency Code
TFI	Time-Frequency Interleaving
TX	Transmit or Transmitter
UWB	Ultra Wideband

7 Overview

Clause 8 defines the interface signals, their directions and functions.

Clause 9 defines the interface parameters and registers. A recommended mapping for PHY parameters is provided along with the register map for PHY registers and setup and hold timing for register access.

Clause 10 defines the frame formats for data exchanges over the interface.

Clause 11 is the Theory of Operation for the complete interface covering the PHY states and transitions, reset and sleep protocols, frame timing references, preamble control and transmit and receive operations for both single frame and burst mode operation as well as receive error cases. The section is completed by definition of the CCA and Management interface protocols.

There are two annexes to this specification. Annex A provides an Electrical Interface and Annex B defines formats for two managed identifiers.

8 Interface Signal Description

The MAC-PHY signal interface is depicted in Figure 1. It consists of the Data Interface including an 8-bit data bus, the Control Interface, the CCA Interface and the Management Interface. The Data Interface, which is used to transfer data to and from the MAC, operates differently depending on the state of the PHY. The Control Interface is used by the MAC to control the operating state of the PHY and by the PHY to indicate TX/RX status to the MAC. The CCA Interface is used for Clear Channel Assessment status indication. The Management Interface is used to access the PHY registers.

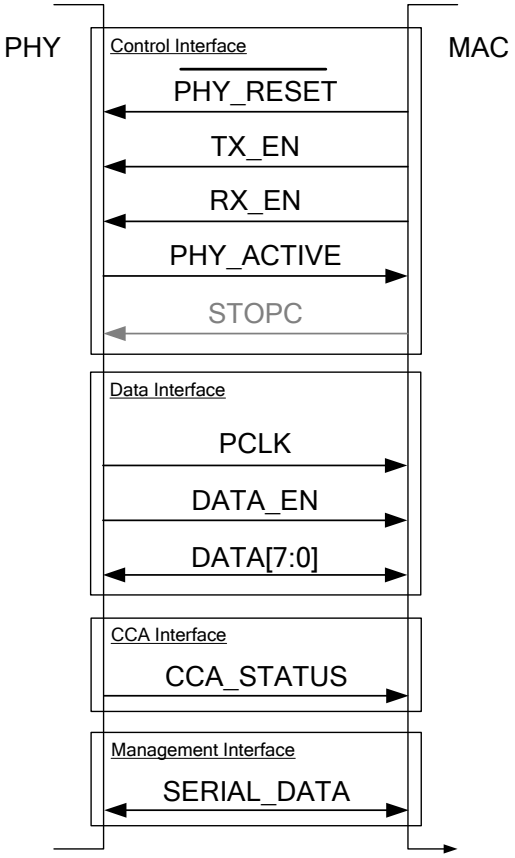

Figure 1 - PHY-MAC interface signals

Table 1 Table 2, Table 3 and Table 4 define the signals in the Control Interface, Data Interface, CCA Interface and Management Interface, respectively. The operational mode of the Data Interface in each PHY state is summarized in Table 5.

8.1 Interface Signal Definitions

8.1.1 Control Interface

Table 1 - Control Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
!PHY_RESET	1	MAC to PHY	!PHY_RESET is asserted for PHY specific interval PHYResetTime to clear all PHY variables and reset the PHY to its initial state. The PHY writes STANDBY to PMMODE and transitions to STANDBY state after !PHY_RESET is de-asserted and reset operations have completed. !PHY_RESET is asynchronous to PCLK. !PHY_RESET is ACTIVE LOW.
TX_EN	1	MAC to PHY	TX_EN is used to place the PHY in TRANSMIT State. [Its secondary use (with RX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.] TX_EN is synchronous to PCLK except in SLEEP state. TX_EN is ACTIVE HIGH.
RX_EN	1	MAC to PHY	RX_EN is used to place the PHY in RECEIVE State. [Its secondary use (with TX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.] RX_EN is synchronous to PCLK except in SLEEP state. RX_EN is ACTIVE HIGH.
PHY_ACTIVE	1	PHY to MAC	PHY_ACTIVE is used by the PHY to indicate that it is either transmitting or receiving a frame over the air. In TRANSMIT state, the rising edge of PHY_ACTIVE indicates the start of frame at the local antenna and the falling edge indicates that the entire frame has been transmitted over the air. In RECEIVE state, the rising edge of this signal indicates that the start of the preamble has been detected (SyncDelay + the preceding synchronization fields earlier) and the falling edge indicates that the entire frame has been received (PHYActiveDelay earlier) at the local antenna. PHY_ACTIVE is also used in the special cases of Exit from SLEEP and RESET. PHY_ACTIVE is synchronous to PCLK. PHY_ACTIVE is ACTIVE HIGH.
STOPC (optional)	1	MAC to PHY	On/Off signal for PCLK in STANDBY state. PCLK is active when STOPC is de-asserted and not active when STOPC is asserted. STOPC is asynchronous to PCLK. STOPC is ACTIVE HIGH.

8.1.2 Data Interface

Table 2 - Data Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
PCLK	1	PHY to MAC	Interface clock provided by the PHY. Interface signals are synchronous to the rising edge of PCLK (see Annex A). The nominal rate of PCLK is 66MHz.
DATA_EN	1	PHY to MAC	In TRANSMIT state, this signal is used by the PHY to request more data from the MAC. In RECEIVE state, it is used to indicate to the MAC that there is valid data on the DATA[7:0] bus. DATA_EN is synchronous to PCLK. DATA_EN is ACTIVE HIGH.
DATA[7:0]	8	Bi-directional	DATA[7:0] is an 8-bit wide data bus driven by the MAC in TRANSMIT state and by the PHY in all other states including SLEEP. DATA[7:0] is synchronous to PCLK whether driven by the PHY or the MAC. DATA[7:0] ONE is HIGH.

8.1.3 CCA Interface

Table 3 - CCA Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
CCA_STATUS	1	PHY to MAC	The PHY returns CCA_STATUS after a CCA request is initiated by the MAC writing to the CCRE register via SERIAL_DATA. CCA_STATUS is synchronous to PCLK. CCA_STATUS is ACTIVE HIGH.

8.1.4 Management Interface

Table 4 - Management Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
SERIAL_DATA	1	Bi-directional	The MAC writes control and address bits to SERIAL_DATA to initiate register access. SERIAL_DATA is driven by the MAC for Write operations. It is driven by the MAC for control and address parts of Read operations and by the PHY for the data part of Read operations. SERIAL_DATA is synchronous to PCLK. SERIAL_DATA ONE is HIGH.

8.2 PHY Operational State

Table 5 - PHY Readiness State

STATE	DESCRIPTION
RESET	Transitional state in which the configuration parameters are reset to default values. PCLK is undefined (see 11.11.1).
SLEEP	The radio is off. PCLK is off (see 11.11.2).
STANDBY	The radio is off. PCLK is on (unless STOPC is asserted). STANDBY is a higher activity state than SLEE.
READY	Parts of the radio are on. PCLK is on.
TRANSMIT	The PHY Tx paths and the radio transmit path are active. PCLK is on.
RECEIVE	The PHY Rx paths and the radio receive path are active. PCLK is on.

9 Registers

In registers, bit positions that are defined as reserved shall be ignored on reading and set to ZERO on writing.

Two sets of parameters are defined to allow the MAC to control the operation of the PHY and permit information to be provided by the PHY to the MAC.

- STATIC Parameters

  These parameters are fixed for a given instantiation of the MAC and PHY. They can be considered to be constants for the purposes of the definition of the MAC-PHY Interface and their values can be defined in a given PHY data sheet, stored as constants in the system implementation or provided by any other means. The static parameters are defined in Table 6.

- DYNAMIC Parameters

  These parameters may be changed during operation of the system, and affect operation of the PHY. They shall be implemented within the PHY as registers and can be read and/or written (depending on the specific parameter) via the Serial Management Interface. The dynamic registers are defined in Table 7.

9.1 Bit Ordering and Interpretation

All data structures, except where explicitly stated, are defined with the bit order as shown in Figure 4.

Reserved bits shall be ignored on reading and set to ZERO on writing.

9.2 Register Address Spaces

The PHY has 256 addressable 8-bit registers (8-bit address, 8-bit data) divided into 3 regions:

Dynamic Register region defined by this specification: address 00(h)~1F(h)

Optional Static Parameter region defined by this specification: address 20(h)~7F(h)

Vendor Specific Register region for vender defined registers: address 80(h)~FF(h)

9.3 Static Parameter Definitions

Table 6 - Description of Static Parameters

REGISTER	OCTETS	DEFINITION
SupportedRegDomains	2	Supported regulatory regions. Bit set to ONE if supported, ZERO otherwise First Octet Bit Domain [2:0] Reserved [3] European Region [4] United States of America [5] Canada [6] Japan [7] Korea Second Octet Bit Domain [7:0] Reserved
SupportedDataRates	2	Set of supported data rates. Bit set to ONE if supported, ZERO otherwise Bit Data Rate Supported [0] 53,33 Mbps [1] RESERVED [2] 80 Mbps [3] 106,7 Mbps [4] RESERVED [5] 160 Mbps [6] 200 Mbps [7] 320 Mbps [8] 400 Mbps [9] 480 Mbps [15:10] RESERVED
NumChannelsSupported	1	Number of supported channels

Table 6 - Description of Static Parameters (continued)

REGISTER	OCTETS	DEFINITION
SupportedDiversity	1	Number of additional antennas provided for diversity [1:0] Number of additional receive antennas [3:2] Reserved [5:4] Number of additional transmit antennas [7:6] Reserved
SupportedChannels	1	Supported Channels. Bit set to ONE if supported, ZERO otherwise Bit Channel Supported [0] TFC channels in band group 1 supported [1] TFC channels in band group 2 supported [2] TFC channels in band group 3 supported [3] TFC channels in band group 4 supported [4] TFC channels in band group 5 supported [7:5] RESERVED
TXPowerLevel	16	Array of transmit power levels. Each element from 0 to (NumTxPowerLevels-1) of the array holds a supported transmit power. The format of the power level datum is PHY vendor specific. The other elements shall be set to zero. Element 0 shall hold the maximum transmit power supported.
NumTxPowerLevels	1	Number of transmit power levels supported. Permitted range (0..15) with 0 meaning a single fixed power level only. [3:0] number of levels (permitted range 0..15) [7:4] RESERVED
SupportedPHYStates	1	Supported PHY States. Bit set to ONE if supported, ZERO otherwise. [0] SLEEP [1] STANDBY [2] READY [3] TRANSMIT [4] RECEIVE [7:5] RESERVED
PHYClockAccuracy	1	Accuracy of PHY clock. Units ppm.
PHYResetTime	1	Interval during which !PHY_RESET shall be held asserted for the PHY to perform the RESET operation. Units us.

Table 6 - Description of Static Parameters (continued)

REGISTER	OCTETS	DEFINITION
WakeUpDelay	2	Time to transition from SLEEP mode to STANDBY mode. Units 0,5 µs.
TurnOnDelay	2	Radio turn-on time during transition from STANDBY mode to READY mode. Units 0,5 µs.
TxDataDelay	1	Time period before the end of the preamble at the local antenna before which the PHY will not assert DATA_EN to request the first octet of header data. (See 11.4) Units µs.
TxDelay	2	Delay from the rising edge of TX_EN to the time when the PHY feeds the leading edge of the preamble waveform to the antenna. Units ns.
RxDelay	2	Delay from the rising edge of RX_EN to the time when the PHY begins the preamble acquisition processing. Units ns.
Tx2RxDwellTime	2	Minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion. Units ns.
Rx2TxDwellTime	2	Minimum interval between RX_EN de-assertion and TX_EN assertion. Units ns.
SyncDelay	2	Delay from the end of the last symbol of the Frame Synchronization Sequence of the preamble waveform in the local antenna to the time when the PHY asserts PHY_ACTIVE. Note that since the preamble arrives asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be asserted assuming optimal alignment of the received preamble and PCLK. Units ns.
TxSetupTime	2	Minimum time between setting of transmit control registers and assertion of TX_EN. Units PCLK cycles.
RxSetupTime	2	Minimum time between setting of receive control registers and the assertion of RX_EN or de-assertion of PHY_ACTIVE. Units PCLK cycles.
TxHoldTime	2	Minimum time between the assertion of TX_EN and changing transmit control registers for the next frame. Units PCLK cycles.
RxHoldTime	2	Minimum time between the assertion of RX_EN or deassertion of PHY_ACTIVE and changing receive control registers for the next frame. Units PCLK cycles.
PHYID	2	PHY identifier to specify vendor, product and version. See Annex B for format and coding.

Table 6 - Description of Static Parameters (concluded)

REGISTER	OCTETS	DEFINITION
PHYVersion	1	Edition of the ECMA-368 PHY specification supported. See Annex B for format and coding.
PHYActiveDelay	2	Delay from the end of the last symbol of the frame received in the local antenna and PHY_ACTIVE de-assertion. Note that since received frames arrive asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be de-asserted assuming optimal alignment of the received frame and PCLK. Units ns.
CCAValidTime	1	Interval following the MAC setting CCRE = ONE after which the PHY should respond with the CCA measurement result. Units 0,5 µs.
MinPTChangeLength	1	Minimum MAC Frame Payload length for the preamble type of the next frame to be different to the current frame. Fixed value = 1 octet
RangingSupported	1	Support of ranging [0] Set to ONE if supported, otherwise set to ZERO [1] Support for 528MHz precision (Mandatory) [2] Support for 1 056MHz precision [3] Support for 2 112MHz precision [4] Support for 4 224MHz precision [5] Support for RANGINGTIMER [23:16] [6] Support for RANGINGTIMER [31:24] [7] RESERVED
RANGING_TRANSMIT_ DELAY	2	The time from the generation of the ranging reference signal (start of the Channel Estimation sequence of the preamble), triggering the RANGINGTIMER capture, to the time this signal reaches the device antenna. Units 1 / 4 224 MHz - same as RANGINGTIMER (see Table 7)
RANGING_RECEIVE_ DELAY	2	The time from the arrival of the reference signal at the antenna to the time this signal is first detected in the PHY, triggering the RANGINGTIMER clock capture. Units 1 / 4 224 MHz - same as RANGINGTIMER (see Table 7)

9.4 Static Parameter Coding

If the values of the static parameters are stored in the PHY, they should be implemented as read only values using the addresses and formats shown in Figure 2 and Figure 3.

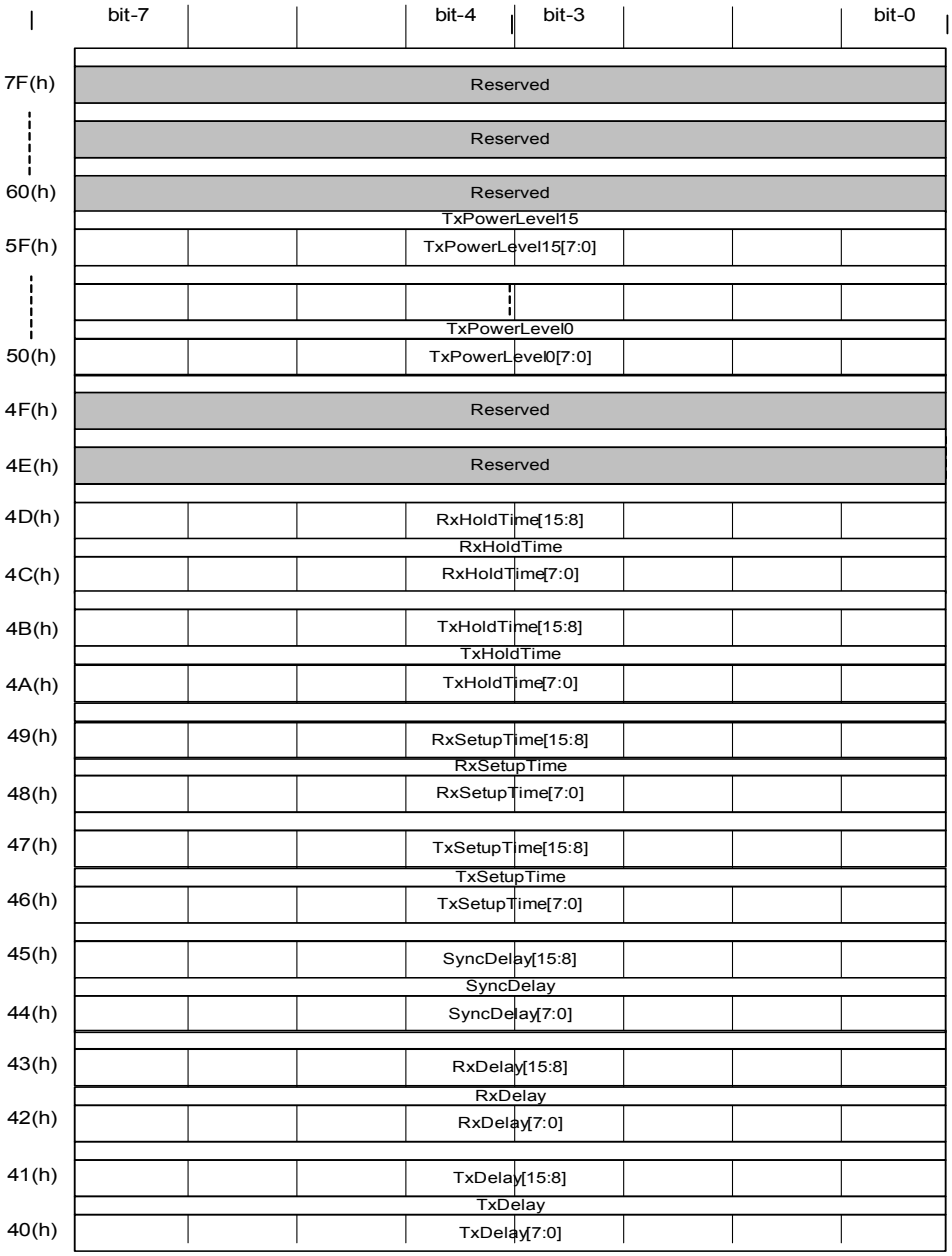

Figure 2 - Static Parameter Encoding 40(h) -7F(h)

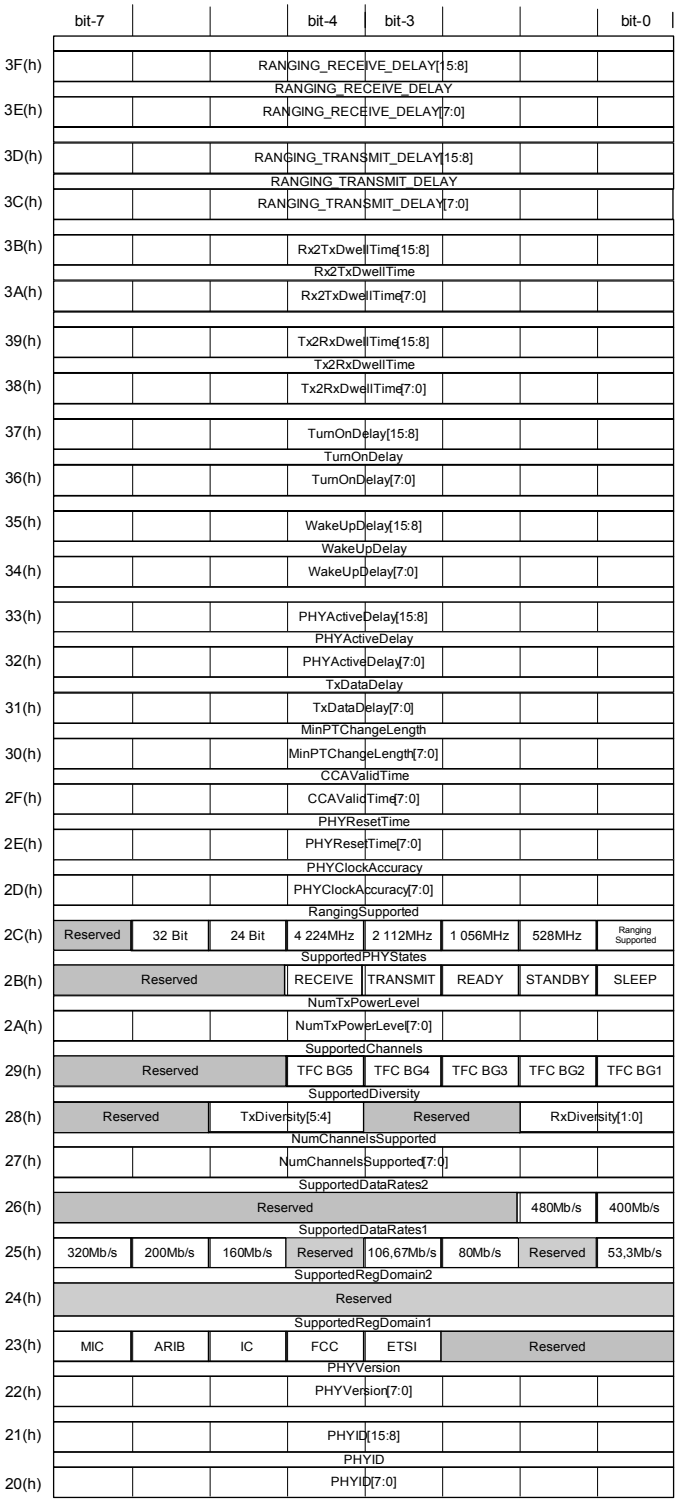

Figure 3 - Static Parameter Encoding 20(h) - 3F(h)

9.5 Dynamic Register Definitions

All registers in the Dynamic Register area are readable (R) and writable (W) by the MAC except RDY in the CONTROL register and RANGINGTIMER which are Read Only.

NOTE
Although the Current Regulatory Domain (CRD) register is both readable and writable, the end-user should not be given the ability to change the contents at will. Some regulatory regions may have strict requirements in this regard.

Table 7 - Description of Dynamic Registers

Addr.	Register	R/W	Description	Init.
00(h)	CONTROL	R/W (Except RDY which is R)	PHY Control register [0] RDY - Result of !PHY_RESET ZERO = Normal completion of initialization ONE = Abnormal completion of initialization [1] Reserved [2] RNGEN ZERO = Ranging disabled ONE = Ranging enabled [3] CCRE – CCA Request ZERO = Stop CCA estimation ONE = Start CCA estimation [7:4] RESERVED	0(h)
01(h)	CRD	R/W	[2:0] RESERVED [7:3] CRD – Current regulatory domain Each domain is mapped to a bit in the register, as follows: Bit Domain 3 European Region 4 United States of America 5 Canada 6 Japan 7 Korea	0(h)
02(h)	TXCHAN	R/W	[5:0] TXCH - Channel of next transmitted frame [7:6] RESERVED (NOTE TXCH is coded as (3-bit Band Group | 3-bit TFC) (See 11.2 of ECMA-368 for the mapping of Channel Number to Band Group and TFC)	0(h)

Table 7 - Description of Dynamic Registers (continued)

Addr.	Register	R/W	Description	Init.
03(h)	TXCTL	R/W	Transmit Control [0] TXPT – Preamble type of next transmitted frame. ZERO = Standard Preamble ONE = Burst Preamble [1] Reserved [3:2] TXANT – Transmit antenna to be used. Value 0..SupportedDiversity[5:4] where: 00 identifies transmit antenna 1 01 identifies transmit antenna 2 10 identifies transmit antenna 3 11 identifies transmit antenna 4 [7:4] TXPWR – Index into TxPowerLevels for transmit power level	0(h)
04(h)	RXCHAN	R/W	Receive Channel [5:0] RXCH - Channel of next received frame [7:6] RESERVED (See 11.2 of ECMA-368 for the mapping of Channel Number to Band Group and TFC)	0(h)
05(h)	RXCTL	R/W	Receive Control [0] RXPT - Preamble type of next received frame ZERO = Standard Preamble ONE = Burst Preamble [1] PTON (R/W) ZERO = PHY does not process PT bit in PLCP header ONE = PHY does process PT bit in PLCP header [3:2] RXANT – Receive antenna to be used. Value 0..SupportedDiversity[1:0] where: 00 identifies receive antenna 1 01 identifies receive antenna 2 10 identifies receive antenna 3 11 identifies receive antenna 4 [7:4] RESERVED	0(h)

Table 7 - Description of Dynamic Registers (concluded)

Addr.	Register	R/W	Description	Init.
06(h)	PMMODE	R/W	[2:0] Power management mode. Values: 0 READY 1 STANDBY 2 SLEEP 3-7 RESERVED [7:3] RESERVED	1(h)
07(h) – 0A(h)	RANGINGTIMER	R	Ranging Timer (units 1 / 4 224MHz) [31:0] RANGINGTIMER – 32-bit ranging counter value Note that this register requires multiple read operations (07(h) to 0A(h)) to retrieve the full value.	0(h)
0B(h)	CRDExtension	R/W	Extension for 2nd Octet of Regulatory domains [7:0] RESERVED	0(h)

9.6 Register Map

Figure 4 shows the register map. Gray portions in the map are reserved.

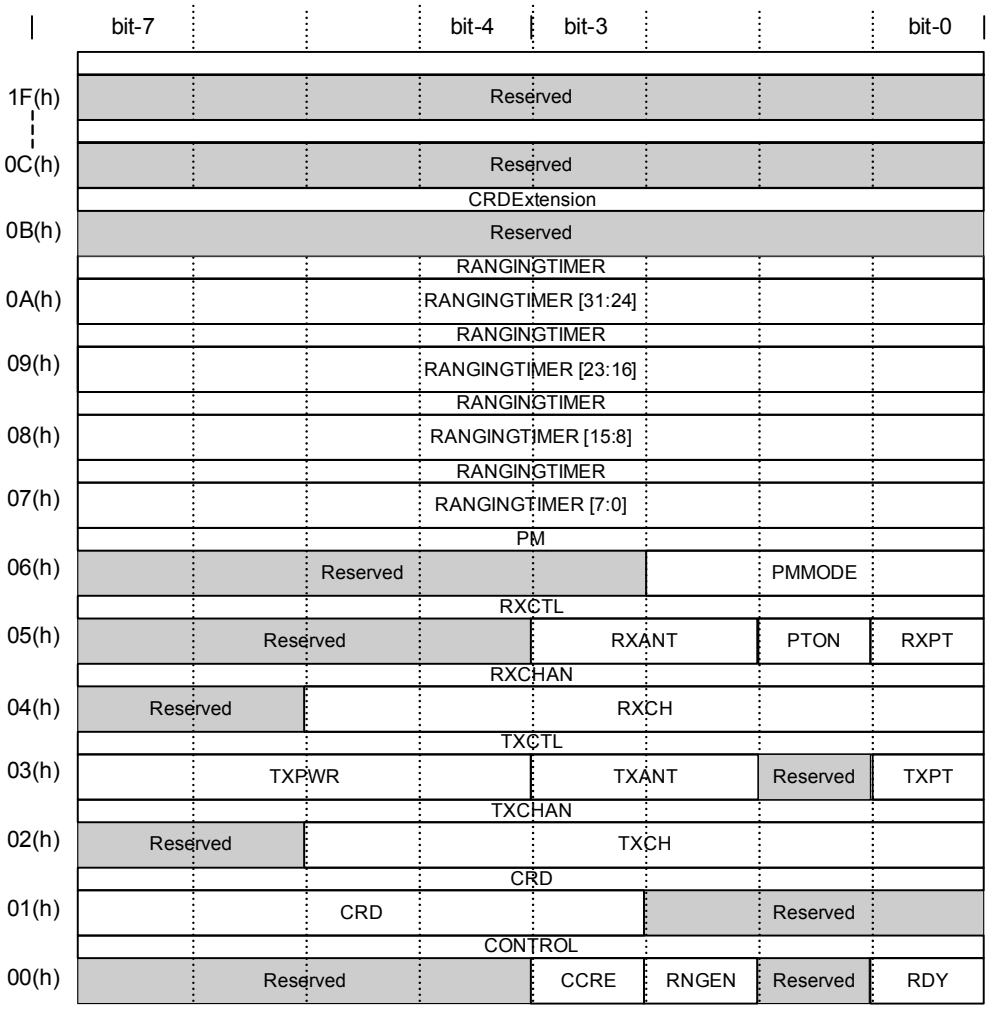

Figure 4 - Register Map

9.7 Register Set Access Timing

9.7.1 Transmit Control Registers

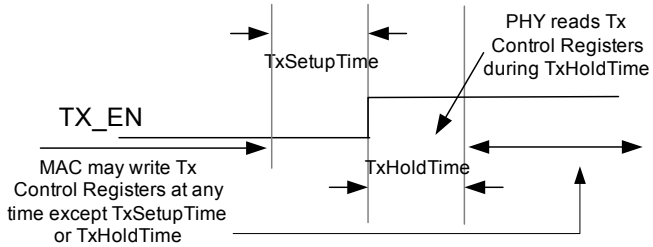

Figure 5 - Transmit Control Register Setup & Hold

TXCHAN and TXCTL (TXPT, TXANT and TXPWR) are registers used to specify parameters for the next transmit frame operation. They shall be set by the MAC at least TxSetupTime PCLK cycles before the assertion of TX_EN and are held stable for at least TxHoldTime PCLK cycles. The PHY shall read these registers within this TxHoldTime period. The values of these registers then control the parameters for the transmit frame operation corresponding to this TX_EN assertion.

9.7.2 Receive Control Registers

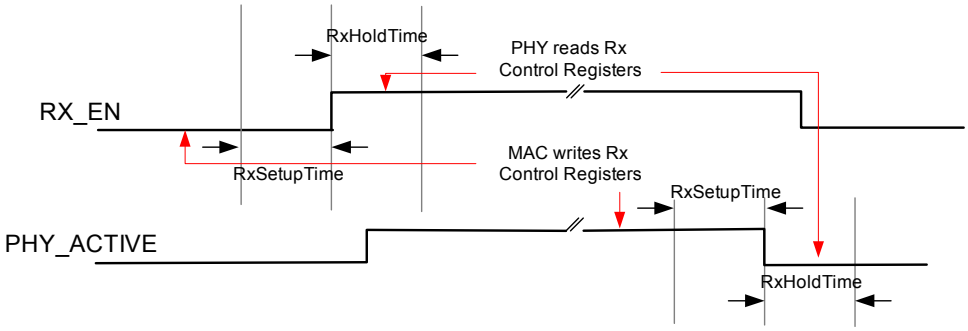

Figure 6 - Receive Control Register Setup & Hold

RXCHAN and RXCTL (RXPT and RXANT) are registers used to specify parameters for the next receive frame operation. They shall be set by the MAC at least RxSetupTime PCLK cycles before the assertion of RX_EN and are held stable for at least RxHoldTime PCLK cycles. The PHY shall read these registers in this RxHoldTime period ignoring any PTON setting and any previous BM or PT settings. The values of these registers then control the parameters for the receive frame operation corresponding to this RX_EN assertion.

For burst mode reception, the MAC shall set the registers for the next receive frame operation at least RxSetupTime PCLK cycles before PHY_ACTIVE de-assertion indicating the end of frame reception. The PHY shall read the registers within RxHoldTime PCLK cycles following the de-assertion of PHY_ACTIVE. These registers then control the parameters for the reception of the next frame if RX_EN is not de-asserted. In receive burst mode (see 11.8.3) PTON together with the BM and PT bits of the preceding frame's PLCP header may override the RXPT register setting.

RX_EN de-assertion and re-assertion has precedence over PHY_ACTIVE de-assertion and will cause the PHY to overwrite any internal values loaded from the receive control registers.

Table 8 - Register Access Parameter Values

Parameter	Minimum Value (PCLK Periods)	Maximum Value (PCLK Periods)
TxSetupTime	0	128
TxHoldTime	0	128
RxSetupTime	0	128
RxHoldTime	0	128

10 Frame Structures

According to the ECMA-368 specification, data is transmitted and received least-significant bit first (bit zero octet zero … bit 7 octet zero, bit 0 octet 1 … bit 7 octet 1 etc.). Consequently, the PLCP header, as shown in Figure 8, is presented to DATA[7:0] as shown in Figure 7.

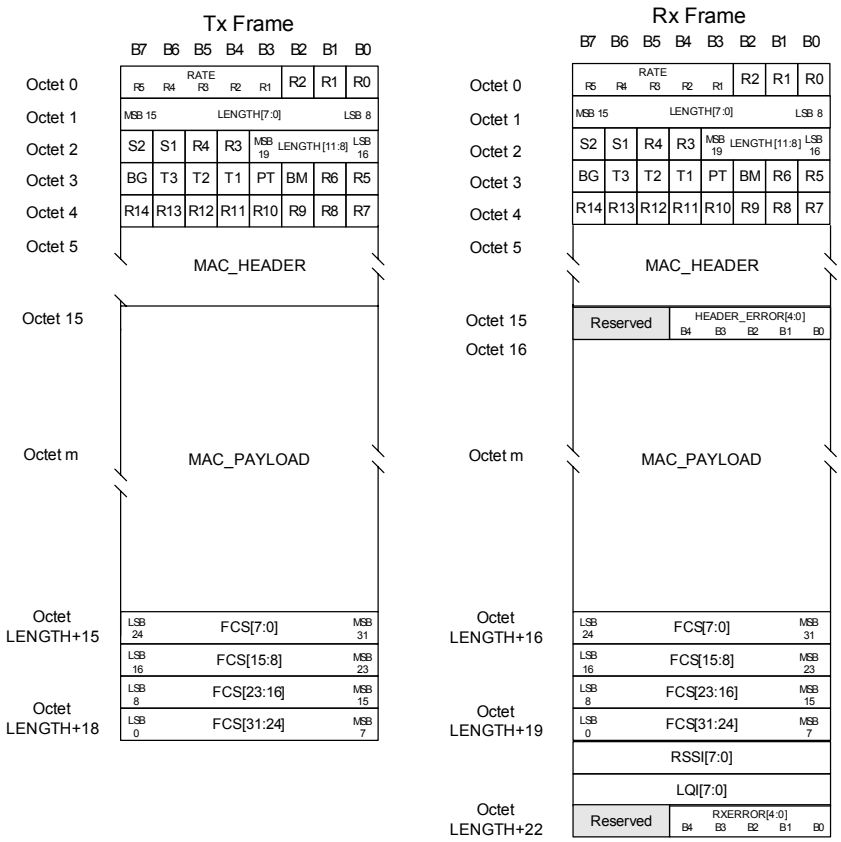

Figure 7 - Frame Structures for Transmit & Receive States

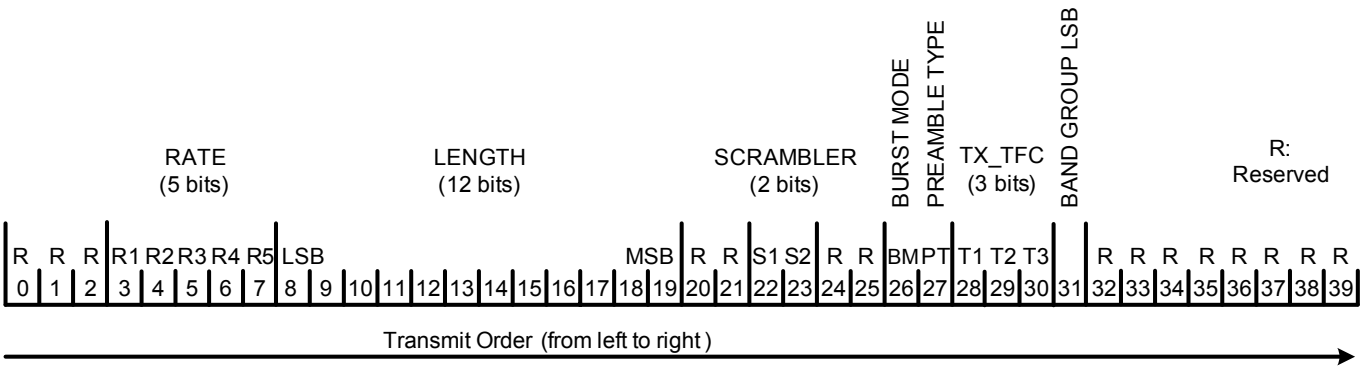

Figure 8 - PLCP Header Format

The MAC_HEADER, MAC_PAYLOAD and FCS are presented to the PLCP as defined in ECMA-368. As defined in that specification, the coefficients ($a_{31..}$ a_0) of the CRC result polynomial :

$$a_{31}x^{31}+ a_{30}x^{30}+ a_{29}x^{29}+ a_{28}x^{28}+ a_{27}x^{27}.....+a_7x^7+ a_6x^6+ a_5x^5+ a_4x^4+ a_3x^3+ a_2x^2+ a_1x+ a_0$$

are mapped to the bits of the FCS as shown in Figure 9 and presented to the PLCP as shown in Figure 7.

bits: b31	b30	b29	…	b2	b1	b0
a0	a1	a2	…	a29	a30	a31

Figure 9 - FCS Field format

Thus when presented to the PLCP least significant octet first (FCS[7:0]) the coefficients of the CRC are transmitted in the order $a_{31..}$ $a_{0.}$

The following TxFrame control bits (see Figure 8) shall be set by the MAC in all transmitted frames and shall be delivered to the MAC by the PHY in the RxFrame format of all received frames:

- RATE is the data rate at which the MAC Frame Payload is transmitted. If LENGTH = 0, RATE shall be set to ‘00000’.
- LENGTH is the MAC Frame Payload length in octets excluding the FCS octets. If LENGTH is zero, the FCS field is not present.
- SCRAMBLER (S1 and S2) is set to ZERO during initialization of the PHY or after any !PHY_RESET. The unsigned binary integer set in SCRAMBLER is incremented by the MAC, modulo 4, for each frame transmitted from the MAC to its PHY.
- BM and PT shall be set in all transmitted fames according to the rules defined in 11.6.
- The MAC sets TX_TFC (T1-T3) and BG as derived from TXCHAN (see Table 7) in all transmitted frames.

Table 9 - TX Frame Fields

<table>
<tr><th>Field</th><th>Bits</th><th>Description</th></tr>
<tr><td>R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14</td><td>1</td><td>RESERVED bits
On TRANSMIT, RESERVED bits SHALL be set to ZERO</td></tr>
<tr><td>RATE</td><td>5</td><td>Indication of transmit data rate of MAC Frame Payload
<table>
<tr><th>Rate (Mb/s)</th><th>R1-R5</th></tr>
<tr><td>53,3</td><td>00000</td></tr>
<tr><td>80</td><td>00001</td></tr>
<tr><td>106,7</td><td>00010</td></tr>
<tr><td>160</td><td>00011</td></tr>
<tr><td>200</td><td>00100</td></tr>
<tr><td>320</td><td>00101</td></tr>
<tr><td>400</td><td>00110</td></tr>
<tr><td>480</td><td>00111</td></tr>
<tr><td>Reserved</td><td>01000 - 11111</td></tr>
</table></td></tr>
<tr><td>LENGTH</td><td>12</td><td>Length of MAC Frame Payload in octets
12-bit unsigned binary integer lsb 8 --- msb 19</td></tr>
<tr><td>SCRAMBLER</td><td>2</td><td>Scrambler initialization bits S1 and S2</td></tr>
<tr><td>BM</td><td>1</td><td>Burst Mode bit (Interframe Space following this frame)
ZERO = Normal Mode (SIFS or other)
ONE = Burst Mode (MIFS)
(NOTE
SIFS = pSIFS
MIFS = pMIFS
as defined in 11.3 of ECMA-368).</td></tr>
<tr><td>PT</td><td>1</td><td>Preamble type of the frame following this frame
ZERO = Standard Preamble
ONE = Burst Preamble</td></tr>
</table>

Table 9 – TX Frame Fields (concluded)

<table>
<tr><th>Field</th><th>Bits</th><th>Description</th></tr>
<tr><td>TX_TFC</td><td>3</td><td>TF Code used at the transmitter (T1-T3)
<table>
<tr><th>TF Code</th><th>T1-T3</th></tr>
<tr><td>1</td><td>100</td></tr>
<tr><td>2</td><td>010</td></tr>
<tr><td>3</td><td>110</td></tr>
<tr><td>4</td><td>001</td></tr>
<tr><td>5</td><td>101</td></tr>
<tr><td>6</td><td>011</td></tr>
<tr><td>7</td><td>111</td></tr>
<tr><td>Reserved</td><td>000</td></tr>
</table></td></tr>
<tr><td>BG_LSB</td><td>1</td><td>Least-significant bit of the Band Group used at the transmitter
<table>
<tr><th>Band Group</th><th>BG_LSB (BG)</th></tr>
<tr><td>1, 3, 5</td><td>ONE</td></tr>
<tr><td>2, 4</td><td>ZERO</td></tr>
</table></td></tr>
<tr><td>MAC_HEADER</td><td>80</td><td>MAC Frame header</td></tr>
<tr><td>MAC_PAYLOAD</td><td>---</td><td>Frame Data</td></tr>
<tr><td>FCS</td><td>32</td><td>Frame FCS</td></tr>
</table>

Table 10 - RX Frame Fields

Field	Bits	Description
R0, R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18	1	RESERVED bits On RECEIVE, RESERVED bits SHALL be ignored
RATE	5	Same as Tx Frame Fields
LENGTH	12	Same as Tx Frame Fields
SCRAMBLER	2	Scrambler initialization bits shall be ignored on receive.
BM	1	Burst Mode bit indicates the Inter-Frame Space following this receive frame ZERO = Normal IFS (Depends on MAC context) ONE = Burst Mode IFS (MIFS) (NOTE SIFS = pSIFS MIFS = pMIFS as defined in 11.3 of ECMA-368).
PT	1	Preamble Type for the frame following this frame ZERO = Standard Preamble ONE = Burst Preamble
TX_TFC	3	Same as Tx Frame Fields
BG_LSB	1	Same as Tx Frame Fields
MAC_HEADER	80	Same as Tx Frame Fields
HEADER_ERROR	5	Immediate Header Error reporting. Error is indicated by the corresponding bit set to ONE. bit 0: RESERVED bit 1: RESERVED bit 2: RESERVED bit 3: UNSUPPORTED_RATE bit 4: HCS_ERROR All bits = ZERO represents “NO_ERROR”
MAC_PAYLOAD	---	Same as Tx Frame Fields
FCS	32	Same as Tx Frame Fields
RSSI	8	Receive power estimate of received signal
LQI	8	Quality estimate of received signal

Table 10 - RX Frame Fields (concluded)

Field	Bits	Description
RXERROR	5	Receiving results of Rx frame Each bit represents the cause of error bit 0: PAYLOAD_ERROR bit 1: RESERVED bit 2: RESERVED bit 3: UNSUPPORTED_RATE bit 4: HCS_ERROR All bits = ZERO represents “NO_ERROR”

11 Interface Theory of Operation

11.1 Overview

A simplified PHY state diagram is shown in Figure 10.

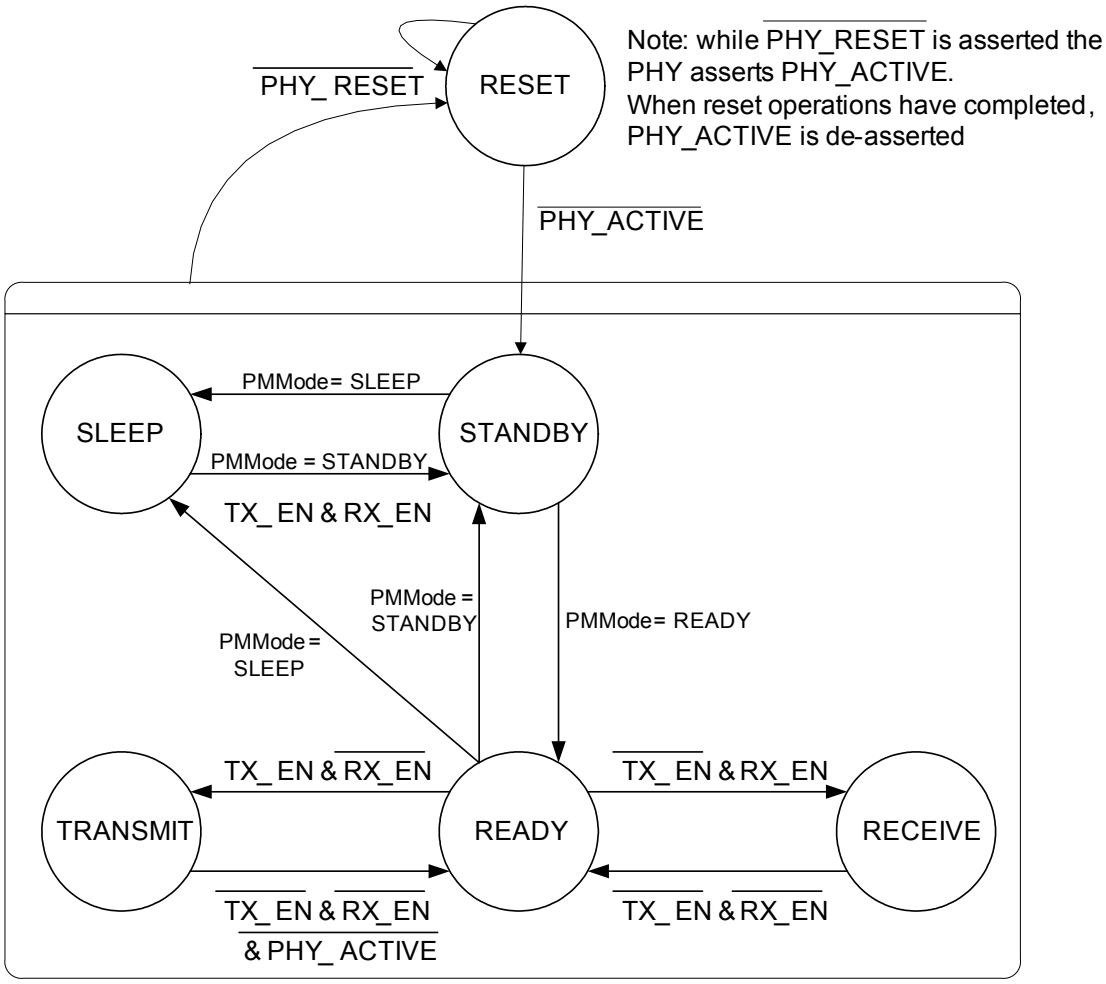

Figure 10 - PHY State Transition Diagram

11.1.1 PHY Reset Protocol

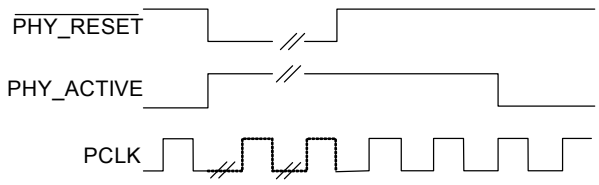

Figure 11 - PHY Reset Protocol

At any time and from any PHY state including after initial power on, the MAC may force the PHY into RESET state by asserting control signal !PHY_RESET. The PHY indicates entry to RESET state by asserting PHY_ACTIVE and optionally stopping PCLK. Transitions on both !PHY_RESET and PHY_ACTIVE in this case are asynchronous to PCLK.

During reset, the PHY drives CCA_STATUS, DATA_EN and DATA[7:0] to their inactive values. The MAC drives RX_EN, TX_EN and SERIAL_DATA to their inactive values. PHY_ACTIVE is driven as described above.

The MAC maintains !PHY_RESET asserted for at least PHY specific interval PHYResetTime. After !PHY_RESET is de-asserted the PHY completes its reset operations. When PCLK is stable (according to PHY specific conditions) the PHY de-asserts PHY_ACTIVE to indicate transition to STANDBY state. The PHY is responsible for setting PMMODE to STANDBY and RDY to the appropriate value. If RDY is set by the PHY to indicate abnormal completion of RESET operation, the meaning of all registers except RDY is undefined.

11.1.2 Exit from Sleep State

The MAC may place the PHY into SLEEP state by writing SLEEP to the PMMODE register (see Table 7). During SLEEP state, the PHY reduces power consumption by turning unnecessary functions off. However, the contents of the Dynamic Registers are maintained through SLEEP and can be assumed unchanged after the PHY is returned to STANDBY state.

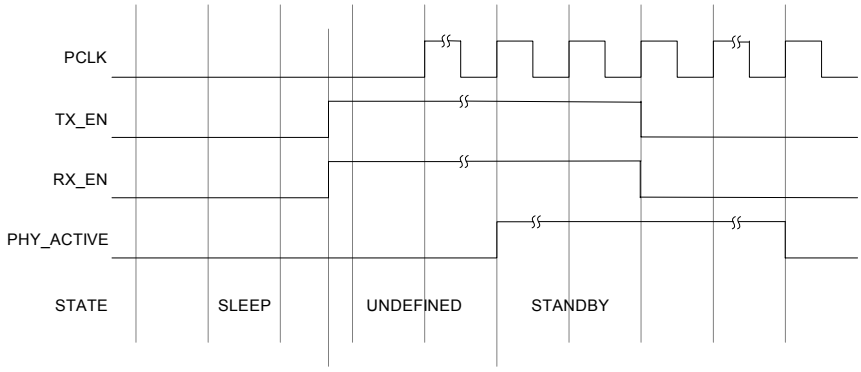

Figure 12 - Exit SLEEP protocol

Exit from SLEEP state is carried out by the following operations:

- The MAC asserts both TX_EN and RX_EN
- When the PHY has reached STANDBY state, it asserts PHY_ACTIVE and sets PMMODE to STANDBY
- When the MAC detects the rising edge of PHY_ACTIVE, it de-asserts TX_EN and RX_EN
- The PHY responds by de-asserting PHY_ACTIVE.

11.1.3 Normal Operation

By writing to the PHY configuration register PMMODE (see Clause 9), the MAC controls transitions between any two of the three PHY states: SLEEP, STANDBY and READY except for transitions from SLEEP state which requires a special operation as described in 11.1.2.

When the PHY is not actively transmitting or receiving, it will be in STANDBY state. In preparation for an active time period, the MAC must first put the PHY in READY state by writing into configuration register PMMODE. The MAC must put the PHY in READY state at least TurnOnDelay microseconds before commanding the PHY into TRANSMIT or RECEIVE state. After this delay, TRANSMIT or RECEIVE state can be initiated by the MAC asserting TX_EN or RX_EN respectively. The PHY is returned to READY state by de-asserting the same signal. (For complete transition conditions, see Transmit and Receive clauses.) Once the PHY is back in READY state, the MAC may either initiate another frame transmission or reception by again asserting TX_EN or RX_EN, or it may command the PHY back into STANDBY by writing to register PMMODE.

Table 11 gives the conditions for the PHY state transitions.

Table 11 - State Transition Conditions

TRANSITION	TX_EN	RX_EN	WRITE TO PMMODE
RESET → STANDBY	LOW	LOW	—
STANDBY → SLEEP	LOW	LOW	SLEEP
SLEEP → STANDBY	HIGH	HIGH	—
STANDBY → READY	LOW	LOW	READY
READY → SLEEP	LOW	LOW	SLEEP
READY → STANDBY	LOW	LOW	STANDBY
READY → TRANSMIT	Rising edge	LOW	—
TRANSMIT → READY	Falling edge	LOW	—
READY → RECEIVE	LOW	Rising edge	—
RECEIVE → READY	LOW	Falling edge	—

11.2 Frame Timing

Precise frame timing is provided by the MAC (except when in Burst Mode as described in 11.7.3) for transmit operations and by the PHY/MAC for receive operations.

The start of the transmitted frame is indicated by the rising edge of TX_EN associated with the PHY-dependent, but fixed, PHY transmit processing delay TxDelay for single frame transmission and for the 1st frame of a Burst transmission.

The end of the transmit frame is indicated by the falling edge of PHY_ACTIVE.

The start of the receive frame is indicated by the rising edge of PHY_ACTIVE associated with the PHY-dependent, but fixed, PHY receive processing delay SyncDelay.

The end of the receive frame is indicated by the falling edge of PHY_ACTIVE associated with the PHY-dependent, but fixed, PHY receive delay PhyActiveDelay.

11.3 Ranging Support

Ranging estimation may be optionally supported by the PHY. Capabilities are indicated by static parameter RangingSupported. If ranging is supported, timing of transmission and reception events may be controlled via the RNGEN bit [2] in the CONTROL [00h] dynamic parameter register.

PHYs which support ranging must provide up to a 32-bit ranging counter and indicate the precision of the timestamp by reference to the frequency of the ranging counter.

RNGEN indicates whether the PHY should set the RANGINGTIMER register from the ranging counter during transmission and reception.

The interface events associated with these timestamps are:

- The start of transmission of the preamble at the local antenna as indicated by the assertion of PHY_ACTIVE
- The acquisition of the preamble as indicated by the assertion of PHY_ACTIVE during reception.

These transitions on PHY_ACTIVE provide support for ranging procedures which may be implemented within or above the MAC by indicating when ranging timestamps should be retrieved. However, the ranging timestamp value is not tied to the PCLK timing associated with PHY_ACTIVE transitions. See 14.2 and 14.5 of ECMA-368 for a definition of the ranging timestamp reference and the associated calibration parameters RANGING_TRANSMIT_DELAY and RANGING_RECEIVE_DELAY.

The processing of the timestamps by the MAC or higher layer functions is outside the scope of this specification. The Two-Way Time Transfer range measurement mechanism defined in 17.15 of ECMA-368 uses the following MAC-PHY interface registers and parameters:

- RANGINGTIMER;
- RangingSupported,
- RANGING_TRANSMIT_DELAY,
- RANGING_RECEIVE_DELAY;
- PHYClockAccuracy.

Calculations are described in Annex H of ECMA-368.

11.4 Transceiver Delay Definitions

Figure 13 and Figure 14 show the principle transceiver delay intervals for Transmit and Receive cases respectively.

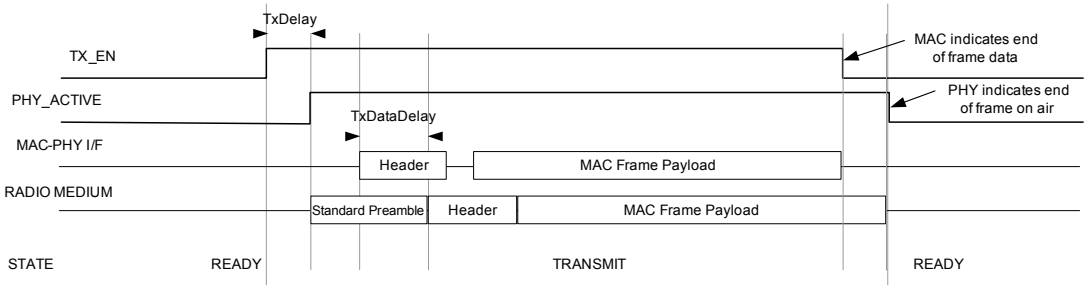

Figure 13 - Transmit Delay Intervals

TxDelay is the interval between the assertion of TX_EN and the start of the first symbol of the preamble being present at the local antenna.

The PHY requests header data by asserting DATA_EN no earlier than TxDataDelay before the end of the preamble as shown in Figure 13. TxDataDelay is measured backwards from the end of the preamble to provide a fixed, preamble independent, header processing interval for PHY implementations and a fixed interval between TX_EN assertion and the first assertion of DATA_EN to be used by the MAC for end of previous frame processing.

The MAC must drive valid data to DATA[7:0] 2 PCLK periods after DATA_EN is asserted.

The PHY de-asserts PHY_ACTIVE on the rising edge of the PCLK following the transmission of the end of the last symbol of the frame at the local antenna.

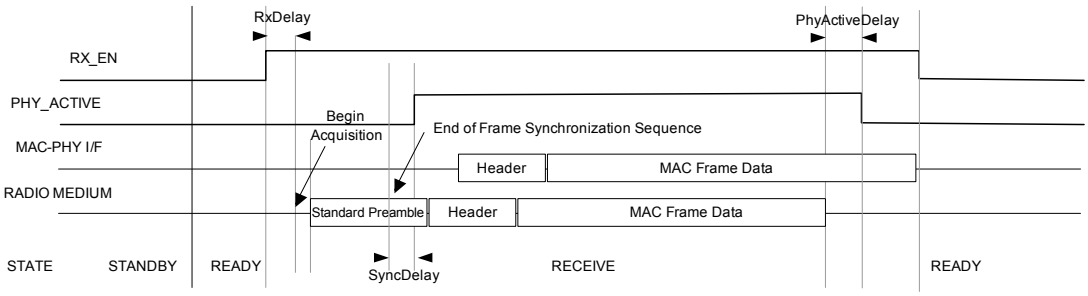

Figure 14 - Receive Delay Intervals

RxDelay is the interval between the assertion of RX_EN and the start of the preamble acquisition operation by the PHY.

Precise start of frame timing is provided by the PHY via the assertion of PHY_ACTIVE a PHY-dependent, but fixed, delay, SyncDelay, after the end of last symbol of the preamble Frame Synchronization Sequence (preceding the Channel Estimation Sequence) arrives at the local antenna.

End of frame timing is provided by de-assertion of PHY_ACTIVE a PHY-dependent, but fixed, delay, PHYActiveDelay, after the end of the last symbol is received at the local antenna. PHYActiveDelay compensates for the processing delay inherent in the PHY receive processing path.

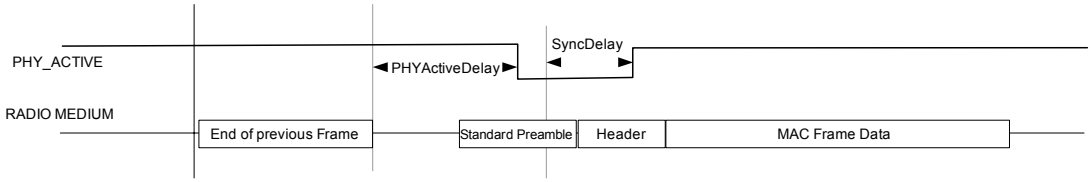

Figure 15 - PHYActiveDelay Timing

As shown in Figure 15, PHYActiveDelay may overlap with the start of the preamble of the next receive frame but must permit PHY_ACTIVE to be de-asserted before the end of the Frame Synchronization sequence to permit acquisition of the incoming frame to be signalled. It is the responsibility of the PHY vendor to specify the value of PHYActiveDelay such that this condition can be met for a zero length frame.

Precise end of frame timing can also be calculated from the known precise start of frame timing, preamble, PHY Header and MAC Frame Data structures, data rates and symbol encoding.

11.5 Transceiver Turnaround Times

11.5.1 RX-TX Turnaround Time

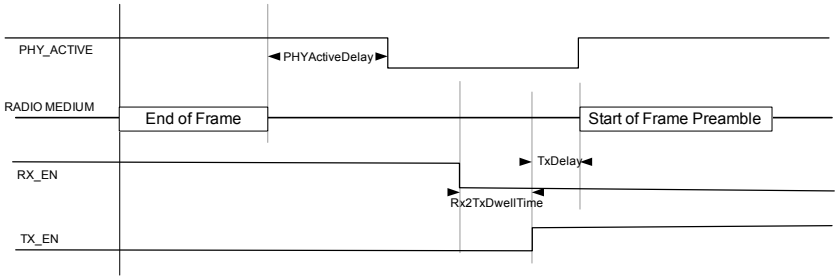

Figure 16 - Rx-Tx Turnaround Time

The minimum interval between RX_EN de-assertion and TX_EN assertion shall be a fixed, PHY specific value, Rx2TxDwellTime. The following inequality shall be respected:

PHYActiveDelay + Rx2TxDwellTime + TxDelay < pSIFS

11.5.2 TX-RX Turnaround Time

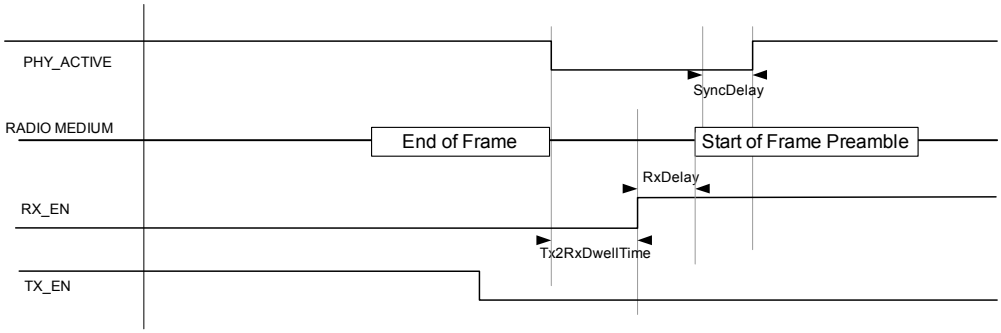

Figure 17 - Tx-Rx Turnaround Time

The minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion shall be a fixed, PHY specific value, Tx2RxDwellTime. The following inequality shall be respected:

Tx2RxDwellTime + RxDelay < pSIFS

11.6 PREAMBLE CONTROL

11.6.1 Single Frame Transmission and Reception

In each single frame transmission the Standard Preamble shall be used.

BM shall be set to ZERO for single frame transmission.

PT shall be set to ZERO for single frame transmission.

In single frame reception, the preamble to be acquired by the receiver is defined by register RXPT which must be set, respecting the receive setup and hold times defined in 9.7.2, to indicate the Standard Preamble.

11.6.2 Burst Mode Transmission

A burst is defined as a MIFS separated sequence of frames (see 11.7.3). In burst transmission, the PHY ensures the accurate MIFS timing between frames. The preamble to be transmitted with each frame is defined by the rules summarized below:

- BM shall be set to ONE for Burst Mode frame transmission.

11.6.2.1 Data Rates of 200 Mbps or Lower

For DATA RATES of 200 Mbps or lower, all frames in the burst shall use the Standard Preamble.

- PT shall be set to ZERO for data rates of 200 Mbps or lower.

11.6.2.2 Data Rates above 200 Mbps

For DATA RATES above 200 Mbps, the first frame in the burst shall use the Standard Preamble. The second and subsequent frames of the burst may use the Burst Preamble or the Standard Preamble.

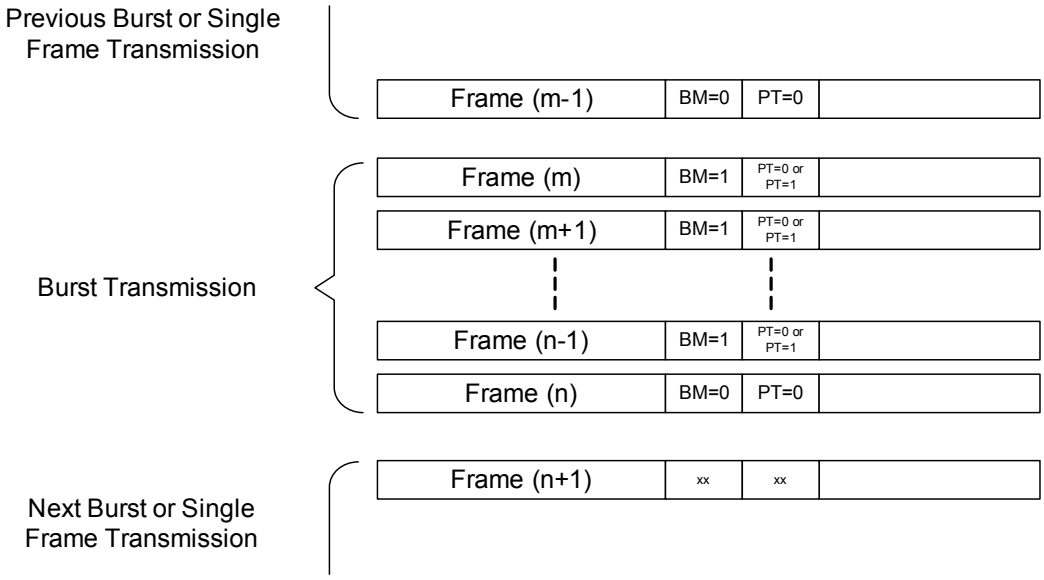

Figure 18 - Burst transmission preamble control

As shown in Figure 18 a burst transmission begins with a frame (m) carrying BM = ONE in the PLCP Header, normally preceded by a frame (m-1) with BM = ZERO and PT = ZERO.

The 1st frame in the burst (frame m) is transmitted with the Standard Preamble.

The 2nd and subsequent frames (m+1,…, n) of the burst are transmitted with a preamble type defined by PT in the preceding (m,…, n-1) frame PLCP Header.

The last frame (n) in the burst is transmitted with BM = ZERO and PT = ZERO.

11.6.3 Burst Mode Reception

In burst mode reception the MAC maintains RX_EN asserted between frames within the burst.

During burst mode reception, processing of PT when BM = ONE is performed automatically by the PHY when register PTON is set to ONE.

The MAC is responsible for all receive preamble control via register RXPT when register PTON is set to ZERO.

A burst mode reception is terminated following reception of a frame with BM = ZERO or immediately after RX_EN is de-asserted.

11.7 Transmit Operation

There are two transmit operations – Single Frame transmit and Burst Mode transmit.

In single frame transmission, a single frame is transferred from the MAC to the PHY and on-air timing is controlled by the state of TX_EN and the PHY transmission of symbols at the local antenna. There is no specific operation following completion of the single frame transmission. The next operation could be another transmit, a receive or a transition to STANDBY.

In Burst Mode Transmit there is an explicit relationship between each frame in a sequence of frames. On-air timing is controlled by TX_EN for the start of the first frame only. Subsequent frame timing is maintained by the PHY during the burst.

11.7.1 Data Bus Ownership

The DATA[7:0] bus is driven by the MAC in TRANSMIT state. The MAC takes control of DATA[7:0] three clocks following TX_EN assertion. The MAC relinquishes control two clocks after TX_EN de-assertion regardless of the PHY requesting data by asserting DATA_EN.

11.7.2 Single Frame Transmission Control

The MAC has complete control over the single frame transmission operation. For each frame transmitted, the MAC sets the PLCP Header parameters listed in Table 12 in the Tx Frame format as defined in Figure 7.

The MAC also sets the Transmit control registers listed in Table 13 respecting the setup and hold times defined in Figure 5.

Table 12 - Single Frame Transmit Parameters

Parameter	Value	Comment
SCRAMBLER	$\|(S1..S2) + 1\|_4$	S1 & S2 are treated as a 2-bit unsigned integer and incremented for each frame sent from the MAC to the PHY.
BM	ZERO	Burst Mode is always ZERO for single frame transmissions.
PT	ZERO	Preamble Type is always ZERO for single frame transmission.
TX_TFC	T1..T3	TFC code used to transmit the frame.
BG_LSB	BG lsb	Least-significant bit of Band Group.
RATE	00000 …. 00111	Encoding of data rate for the MAC Frame Payload part of the frame. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0…4 095	Number of Octets in MAC Frame Payload part of Frame.

Table 13 - Transmit Control Registers for Single Frame Transmit

Register	Value	Comment
TXCHAN	See 11.2 of ECMA-368	Channel on which to perform the transmit operation.
TXCTL-TXPT	ZERO	The preamble is always the Standard Preamble in single frame transmissions.
TXCTL-TXANT	0.. SupportedDiversity[5:4]	Identifies the transmit antenna.
TXCTL-TXPWR	0..NumTxPwrLevels-1	Transmit power level index.
CONTROL-RNGEN	ZERO ONE	If RangingSupported = ZERO, RNGEN is set to ZERO If RangingSupported = ONE RNGEN is set to ZERO to disable RANGINGTIMER setting RNGEN is set to ONE to enable RANGINGTIMER setting.

Figure 19 illustrates the transmission of a single frame, starting from READY state. The MAC starts the transmission by asserting TX_EN while keeping RX_EN low. When the PHY detects the rising edge of TX_EN it transitions to TRANSMIT state, turns on the radio transmit path and begins to transmit the preamble defined by TXPT using its antenna defined by TXANT on the channel defined by TXCHAN.

The timing of TX_EN assertion should be TxDelay ahead of nominal frame timing at the local antenna to compensate for PHY transmit processing delay.

In TRANSMIT State the PHY has full control over data flow. Data is requested from the MAC by asserting DATA_EN at the rising edge of PCLK. The MAC must drive DATA[7:0] 2 clock cycles later.

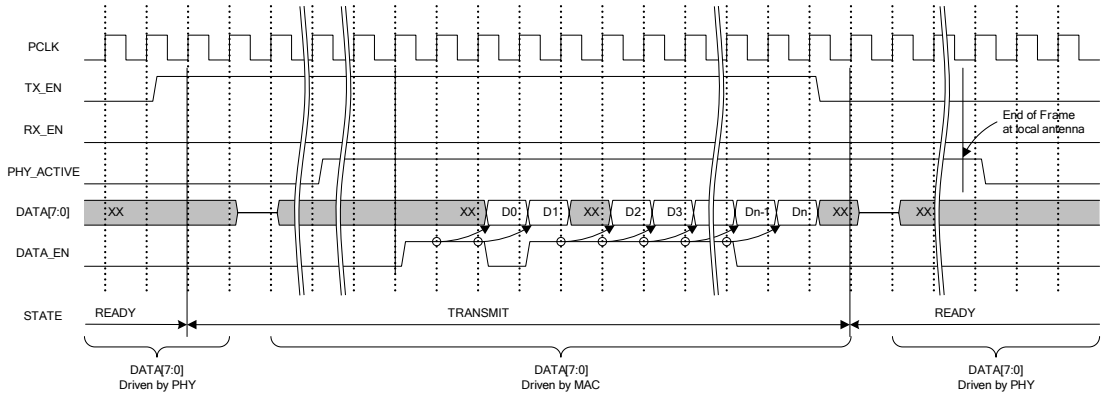

Figure 19 - Single Frame Transmit Timing

The PHY performs the following operations:

- Asserts PHY_ACTIVE at the rising edge of PCLK following the transmission of the leading edge of the first symbol of the preamble at the local antenna.
- If RNGEN = ONE sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in 14.2 of ECMA-368 as the first sample of the first Channel Estimation Sequence of the preamble) according to the precision defined by the RangingSupported static parameter (see Table 7).
- Requests Header and Payload data (as appropriate) from the MAC by asserting DATA_EN while respecting TxDataDelay.

The MAC performs the following operations:

- Transfers one octet of header or payload data (as appropriate) for each request from the PHY via a rising edge of DATA_EN.
- Completes the transmit operation by de-asserting TX_EN at the rising edge of the PCLK cycle after the last octet of the frame FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY.

The PHY completes the single frame transmit operation by:

- De-asserting PHY_ACTIVE at the rising edge of PCLK following the transmission of the trailing edge of the last symbol from the local antenna.
- Transitioning back to READY state.

This procedure is repeated for each transmitted frame. The MAC is responsible for calculating the start of frame timing in all cases.

A frame transmission can be aborted by the MAC at any time by de-asserting TX_EN before the last octet of the FCS (or MAC Header if LENGTH is zero) has been transferred to the PHY (see 11.9).

11.7.3 Burst Mode Transmission Control

A burst is a sequence of MIFS separated frames transmitted from the same source. In burst mode transmission, the MAC has control over the timing of the first frame in the sequence of burst mode frames. The first frame is transmitted in exactly the same manner as a single frame transmission, as described in 11.7.2 except for the PLCP Header parameters listed in Table 14.

Table 14 - Unique Burst Mode PLCP Header Parameters

Parameter	Value	Comment
BM	ONE	Burst Mode must be set to ONE in the first frame of the burst mode sequence.
PT	ZERO ONE	PT = 0 if the next frame will be sent using the Standard Preamble. PT = ONE if the next frame will be sent using the Burst Preamble.
LENGTH	1…4 095	Number of Octets in MAC Frame Payload part of Frame.

Timing for the transmission of subsequent frames in the burst is maintained by the PHY provided that TX_EN is re-asserted within the window shown in Figure 20. The minimum duration TX_EN shall remain de-asserted before re-assertion is three PCLK cycles.

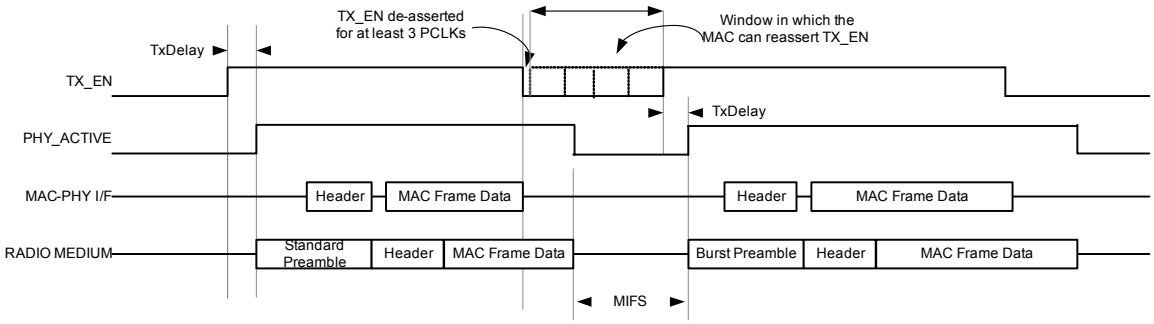

Figure 20 - Burst Mode Transmission

If the MAC re-asserts TX_EN in this window, the PHY assures the start of the first symbol of the preamble of the next frame is presented at the local antenna exactly MIFS after the end of the last symbol of the previous frame. The MIFS interval is defined to be an exact number of symbols to enable the receiver to maintain synchronization from the Burst Preamble.

In burst transmission, the value of PT overrides TXPT in determination of which preamble the PHY transmits ahead of each PLCP header and MAC frame body (if present).

Each subsequent frame in the burst mode sequence is transmitted as in the single frame case except for the PLCP Header parameters in Table 14 and the assurance of the MIFS interval provided TX_EN is re-asserted within the window defined in Figure 20, until the last frame in the sequence which differs in the PLCP parameters define in Table 15.

Table 15 - Unique Final Frame PLCP Parameters

Parameter	Value	Comment
BM	ZERO	Burst Mode must be set to ZERO in the last frame of the burst mode sequence.
PT	ZERO	PT must be set to ZERO in the last frame of the burst mode sequence.
RATE	00000 … 00111	Encoding of data rate for the MAC Frame Payload part of the frame. Value shall be set to 00000 if LENGTH is zero.
LENGTH	0 … 4 095	Number of Octets in MAC Frame Payload part of Frame. Note the special case of a frame with LENGTH of zero is permitted since the MIFS interval will not be used following this frame.

11.7.4 Burst Mode Transmit Error Recovery

If TX_EN is re-asserted:

- later than TxDelay before MIFS, but earlier than MIFS, after the end of the previous frame, the behaviour of the PHY is undefined;
- later than MIFS after the end of the previous frame, the PHY shall abort burst mode transmission and return to normal transmission. The next assertion of TX_EN will be treated as a single frame transmission or the first frame of a new burst mode transmission.

11.8 Receive Operation

11.8.1 Data Bus Ownership

The DATA[7:0] bus is driven by the PHY in RECEIVE state. Valid data is indicated by the rising edge of DATA_EN being asserted at the rising edge of PCLK.

11.8.2 Single Frame Reception Control

The MAC controls frame reception operations via the RX_EN control signal. For each frame received, the MAC sets the Receive control registers listed in Table 16**,** respecting the setup and hold times defined in Figure 6. The PHY reports the received PLCP Header parameters in the receive frame format as described in Figure 7.

Table 16 - Receive Control Registers for Single Frame Receive

Register	Value	Comment
RXCHAN	See 11.2 of ECMA-368	Channel on which to perform the receive operation.
RXCTL-RXPT	ZERO	RXPT is set to ZERO if the PHY should seek to acquire a Standard Preamble. Single frames are always transmitted using the Standard Preamble.
RXCTL-RXANT	0.. SupportedDiversity[1:0]	Identifies the receive antenna.
RXCTL-PTON	ZERO ONE	PTON is ignored for single frame reception.
CONTROL-RNGEN	ZERO ONE	If RangingSupported = ZERO, RNGEN is set to ZERO. If RangingSupported = ONE RNGEN is set to ZERO to disable RANGINGTIMER setting RNGEN is set to ONE to enable RANGINGTIMER setting.

The reception of a single frame is depicted in Figure 21, starting from the READY state. The MAC commands the PHY into RECEIVE state by asserting RX_EN while keeping TX_EN de-asserted.

When the PHY detects the rising edge of RX_EN, it transitions to RECEIVE state, turns on the radio receive path, waits RxDelay and then starts a preamble acquisition as defined by RXPT using its receive antenna defined in RXANT on the channel defined in RXCHAN. RxDelay is the turn-on time for the radio receive path.

The PHY has full control over data flow during frame reception.

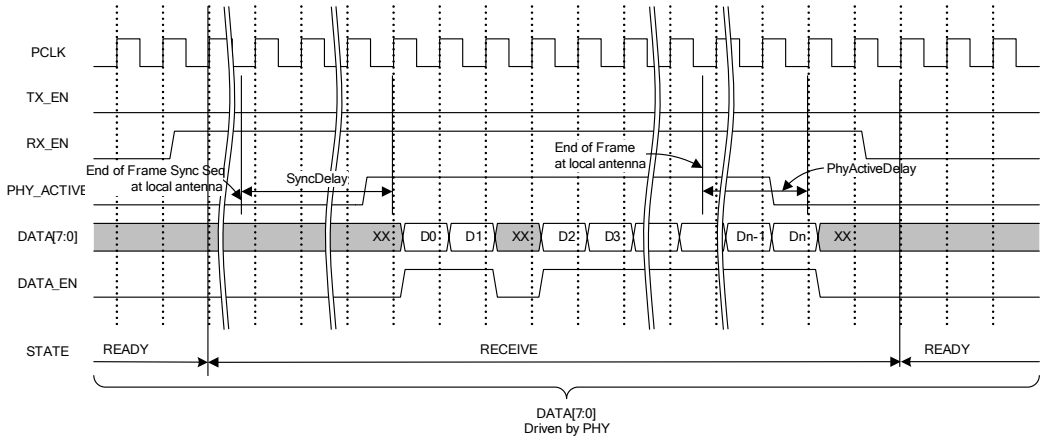

Figure 21 - Single Frame Receive Timing Diagram

The PHY performs the following operations:

- The PHY will seek to acquire the specified preamble on the specified antenna and channel RxDelay after the assertion of RX_EN.

- Preamble acquisition is signalled by the PHY asserting PHY_ACTIVE, as indicated in Figure 21. The delay between the end of the last symbol of the Frame Synchronization Sequence of the preamble (before the Channel Estimation Sequence) in the antenna and the raising edge of PHY_ACTIVE is a PHY-dependent, but fixed, delay SyncDelay.
- If RNGEN = ONE sets Dynamic Register RANGINGTIMER at the Ranging Reference Signal (defined in 14.2 of ECMA-368) according to the precision defined by the RangingSupported static parameter (see Table 7).
- The PHY decodes the received symbols and transfers the PLCP Header to the MAC by the assertion of DATA_EN. At each PCLK rising edge with DATA_EN asserted the MAC reads one octet of data into the RX Frame.
- The PHY interprets the PLCP header parameters and computes the header checksum and compares it with the HCS field in the received PLCP header. The PHY reports the status of the header in HEADER_ERROR as defined in Figure 7.

The MAC performs the following operations on the RX Frame fields:

- Interprets the HEADER_ERROR parameter. If any bit in HEADER_ERROR is set, the MAC should perform frame recovery by de-asserting and re-asserting RX_EN not less than 3 PCLK cycles later
  - If header checksum verification failed, the receive operation is terminated according to 11.11.2.1.
  - If the PLCP header payload RATE is not supported, the PHY terminates the receive operation according to 11.11.2.2.
- Interprets RX Frame field LENGTH – the length in octets of the MAC Frame Payload. The MAC uses this parameter as needed to support the transfer of received data from the DATA[7:0] bus.

The MAC continues the receive operation, if HEADER_ERROR reports no errors, transferring one octet of data for each rising edge of PCLK while DATA_EN is asserted. After LENGTH octets have been received the MAC transfers the 4 octets of the FCS and 3 octets of receive quality information into the receive frame and processes the remaining parameters:

- RX Frame field FCS. The MAC computes the FCS according to its specified CRC algorithm and compares the result with the RX Frame FCS value to determine the validity of the MAC Frame Payload data.
- RX Frame field RSSI – received signal strength indication. The MAC uses this value as required to support links with the transmitting device.
- RX Frame field LQI – link quality indicator. The MAC uses this value as required to support links with the transmitting device.
- RX Frame field RXERROR – receive error status. The MAC interprets any set bit in RXERROR as required to perform frame reception error handling.

If the PHY detects an unrecoverable payload error, the receive operation shall be terminated according to 11.11.2.3.

The PHY completes the receive operation by:

- De-asserting PHY_ACTIVE at the rising edge of PCLK a PHY-dependent, but fixed, delay, PHYActiveDelay, after the trailing edge of the packet waveform at the local antenna.

The MAC completes the receive operation by:

- De-asserting RX_EN. The PHY remains in RECEIVE state until RX_EN is de-asserted by the MAC, at which point it transitions back to READY.

A frame reception can be aborted before completion by de-asserting RX_EN as described in section 11.10.

11.8.3 Burst Mode Reception Control

In Burst Mode reception the receiving MAC commands the PHY to perform continuous frame reception by maintaining RX_EN asserted following reception of a frame with BM set to ONE. Each frame received with BM = ONE is processed in a manner identical to single frame reception except for the de-assertion of RX_EN to complete the reception operation. The frame symbol timing is determined by the transmitter but the receiving PHY can exploit the PLCP header BM and PT fields to improve receive performance.

There is one receive control register specific to burst mode as shown in Table 17.

Table 17 - Unique Burst Mode Receive Registers

Parameter	Value	Comment
RXCTL-PTON	ZERO ONE	When PTON = ZERO, the MAC must control all receive preamble acquisition via RXPT. When PTON = ONE, the PHY interprets the PT field in PLCP headers with BM = ONE.

Following reception of a frame with BM =ONE, the PHY prepares to receive a new preamble exactly MIFS after the end of that frame using the preamble indicated by RXPT if PTON = ZERO, or the preamble indicated by PT if PTON = ONE.

Figure 22 shows a sequence of burst mode received frames with MIFS separation. The timing of each frame is bracketed by the assertion and de-assertion of PHY_ACTIVE with SyncDelay and PhyActiveDelay as in the case of single frame reception.

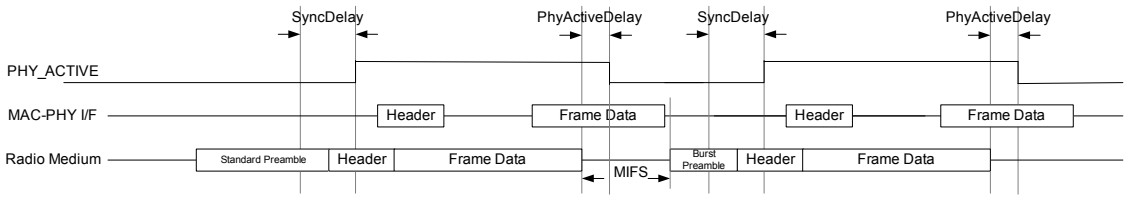

Figure 22 - Burst Mode Receive with MIFS

As long as each received frame carries BM = ONE, the MAC maintains RX_EN asserted and the PHY will continue to perform acquisition and frame reception, each time using the preamble as defined by the previously received PT value or the RXPT value depending on the setting of PTON.

The burst is terminated upon receipt of a frame with BM = ZERO after which the MAC de-asserts RX_EN in an identical manner to that for single frame reception.

11.8.4 Burst Mode Reception Error Recovery

At any time within a burst, the MAC may recover from reception errors and terminate Burst Mode reception by de-asserting RX_EN.

11.8.5 Zero Length Frame Reception

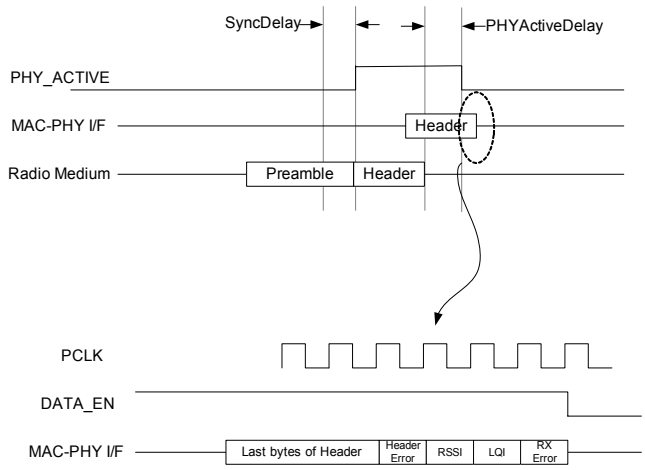

Figure 23 - Zero Length Frame Reception

Figure 23 shows zero length frame reception and presentation of the associated receive parameter block (RSSI, LQI and RXERROR) following the HEADER_ERROR octet.

The receive parameters do not necessarily follow immediately after the HEADER_ERROR octet as the PHY may exploit flow control via DATA_EN when delivering the receive parameter block.

Note that DATA_EN is always used to qualify DATA[7:0] as the PHY retains full flow control during receive operation.

11.9 MAC Transmit Abort

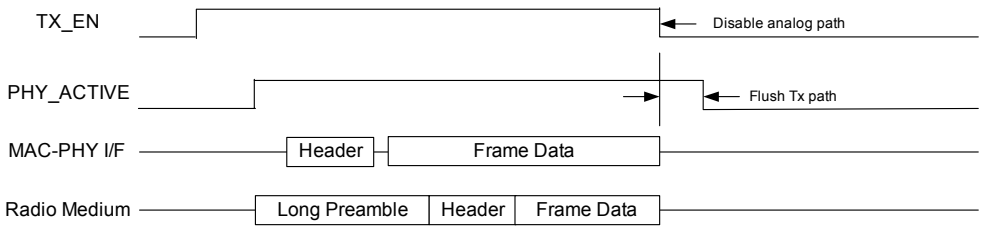

Figure 24 - MAC Aborted Transmit

Figure 24 shows the operation of the interface when the MAC de-asserts TX_EN before delivering the last octet of the FCS to the DATA[7:0] bus.

Upon detecting de-assertion of TX_EN, the PHY shall immediately disable the path to the local antenna so that no further symbols are transmitted but may take the necessary time to flush the transmit logic before de-asserting PHY_ACTIVE at the rising edge of PCLK and returning to READY state.

Note that it is assumed that immediate cessation of transmission at the local antenna is expected to require disabling the analog transmit path. The PHY will normally require additional time to reset the digital transmission path before being ready to resume normal operation.

11.10 MAC Receive Abort

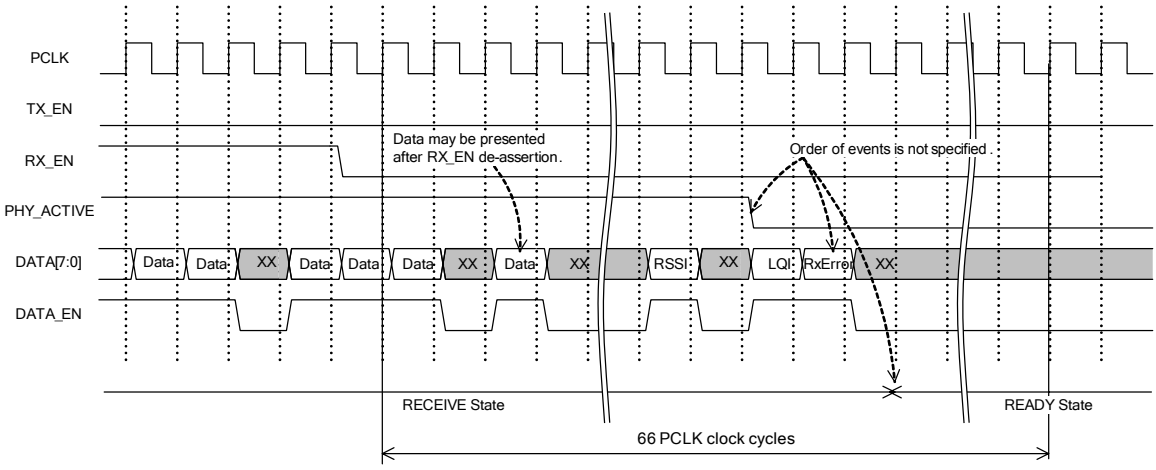

Figure 25 - MAC Aborted Receive Timing Diagram

Figure 25 shows the operation of the interface when the MAC de-asserts RX_EN before the end of frame has been received at the local antenna. Normal RECEIVE operation requires that RX_EN be asserted until after the last octet of the receive parameter block (RXERROR) has been presented to the MAC at the DATA[7:0] bus and validated by DATA_EN.

- The MAC may abort a receive operation at any time after asserting RX_EN by de-asserting RX_EN.

If RX_EN is de-asserted at any time before this last octet transfer, irrespective of whether PHY_ACTIVE is asserted or de-asserted, the following abort operation occurs:

- Within 66 PCLK clock cycles of detecting the de-assertion of RX_EN, the PHY shall abort the receive operation, shall stop transferring data to the MAC, shall present the receive parameter block which will be qualified by DATA_EN and shall de-assert PHY_ACTIVE (if asserted).
- If 19 or more octets of data, including the PHY header, the MAC header and HEADER_ERROR have been delivered by the PHY, the MAC shall consider the last three octets delivered by the PHY within these 66 PCLK clock cycles to be the receive parameter block.
- Otherwise, all data delivered by the PHY for the aborted receive operation is undefined.

The order in which PHY_ACTIVE is de-asserted and the receive parameter block is presented is not specified but must complete within 66 PCLK cycles after de-assertion of RX_EN.

A special case should be noted for Burst Mode. If the acquisition of the next frame is signalled by the assertion of PHY_ACTIVE before the completion of delivery of the data and receive quality block of the preceding frame, de-assertion of RX_EN will abort both the delivery of the preceding frame and the incoming frame.

11.11 Error Conditions

11.11.1 Transmit Error Conditions

There are no defined error conditions that occur during transmit operations.

11.11.2 Receive Error Conditions

11.11.2.1Header Checksum Error

The PHY computes the header checksum (HCS) for the received PHY Header and compares it with the value in the header HCS field. If this check fails, the contents of the header cannot be trusted – including the critical LENGTH parameter that defines the extent of the MAC Frame Payload field.

In this case, the PHY sets the HEADER_ERROR bits in the receive frame data structure. The PHY then behaves as if a zero length frame had been received.

Even though the header checksum fails to validate the header, the Rx Frame will contain the following:

- The PLCP header including the RATE and LENGTH
- The MAC header
- The HEADER_ERROR bits
- RSSI
- LQI
- RXERROR

The PHY shall de-assert PHY_ACTIVE at a suitable interval after detection of the header checksum failure. In this HCS error case, end of frame timing derived from the de-assertion of PHY_ACTIVE is not valid. HEADER CHECKSUM ERROR is set in both HEADER_ERROR and RXERROR fields.

If the MAC maintains RX_EN asserted following the indication of HCS error, the PHY will continue to seek to acquire a frame using the same preamble type used in the frame whose header checksum failed.

If the Preamble type needs to be re-set (e.g. after failure to acquire a Burst Preamble, the MAC may set the preamble to Standard Preamble) the MAC should de-assert RX_EN, set RXPT to the appropriate value and re-start the PHY's acquisition operation by re-asserting RX_EN. It is the MAC's responsibility to determine the timing of re-acquisition following a lost frame, including loss of an intermediate frame in a burst.

11.11.2.2 Unsupported Data Rate

If the data values in the PHY and MAC Header are validated by the HCS but one or more of the parameters is set to an unsupported value (e.g. Data Rate), the PHY sets the HEADER_ERROR bits in the receive frame data structure and performs a zero length frame receive operation as described in 11.11.2.1.

The PHY shall de-assert PHY_ACTIVE at a suitable interval after detection of the unsupported data rate. The corresponding error bits are set in both the HEADER_ERROR and RXERROR fields.

11.11.2.3 Unrecoverable Detected Payload Error

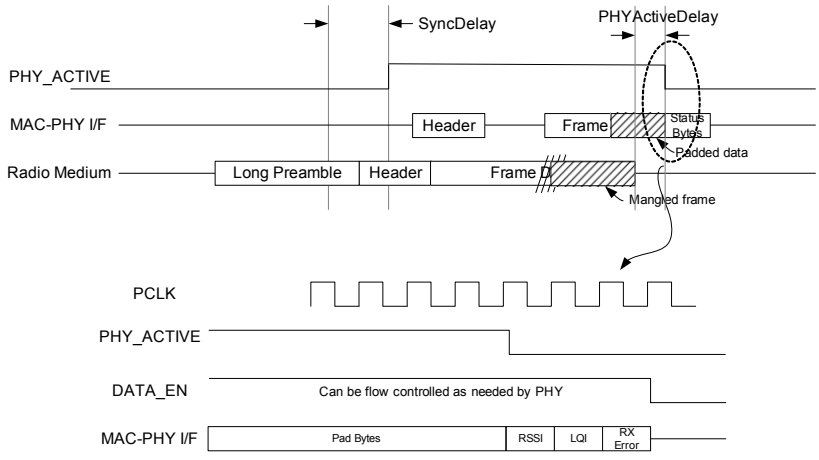

Figure 26 - Unrecoverable Payload Error Handling

Figure 26 shows how an incoming frame aborted by the PHY is signalled after the PHY detects an unrecoverable error while receiving the frame body.

In this case, the PHY can use the content of the PLCP header which has been received with a good HCS. The PHY uses the LENGTH field to determine how many octets of the frame body remain to be transferred to the MAC via the DATA[7:0] bus.

The PHY pads this many undefined value octets at DATA[7:0], qualified by DATA_EN to complete the receive frame operation. PHY_ACTIVE is de-asserted at the nominal end of frame at the local antenna that the PHY computes from LENGTH plus PHYActiveDelay (see Figure 26). The receive quality block is transferred as for a normally completed receive operation.

The PHY sets the PAYLOAD_ERROR bit in RXERROR to signal the aborted receive. In addition, the undefined value pad octets will in general cause the MAC FCS check to fail.

11.12 Clear Channel Assessment

The CCA Interface is used for Clear Channel Assessment status indication. It consists of the CCA_STATUS signal and the following dynamic registers:

Table 18 - CCA Dynamic Registers

Addr.	Register	Bit	Field	R/W	Description	Init.
00(h)	CONTROL	3	CCRE	R/W	The MAC controls CCA estimation by the PHY by writing to CCRE. ZERO Stop CCA Estimation ONE Start CCA Estimation	ZERO

Other Dynamic Registers may be provided in the Vendor Specific Register area for enhanced control of the CCA operation since measurement intervals and detection thresholds are highly dependent on the design of the estimation circuit.

11.12.1 CCA Interface Signals

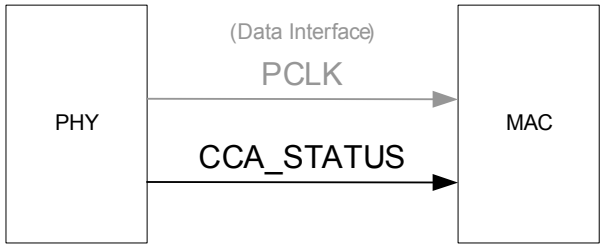

Figure 27 - CCA Interface Signals

Table 19 - CCA Interface Signals

Signal name	Width	Direction	Function
CCA_STATUS	1	PHY-MAC	CCA status. ZERO indicates that the wireless medium is idle. ONE indicates that the medium is busy.

11.12.2 Operation of the CCA Interface

The MAC writes a ONE to the CCRE field of the CONTROL register, using the Management Interface, to initiate a CCA measurement.

CCA_STATUS will be driven after PHY specific but constant interval CCAValidTime according to the implementation dependent CCA estimation algorithm, and will be valid as long as the PHY is not in TRANSMIT, STANDBY or SLEEP state. Estimation will continue as long as CCRE is set to ONE.

The MAC writes a ZERO to CCRE, using the Management Interface, when CCA estimation is no longer required.

All other CCA operations will depend on vendor specific register settings.

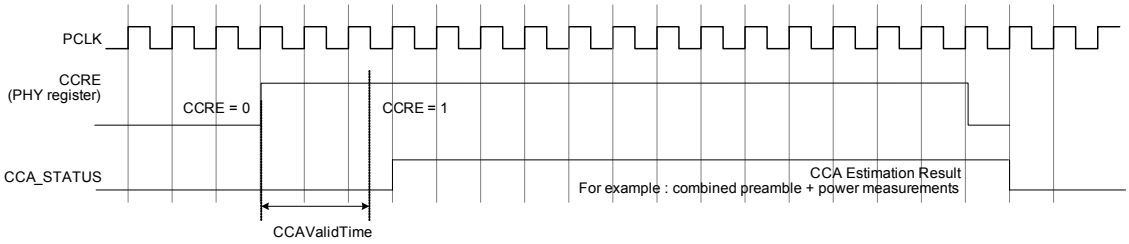

Figure 28 - CCA Operating Timing Diagram

11.13 Management Interface

11.13.1 Management Interface Signals

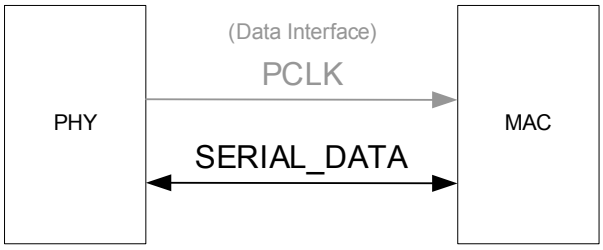

Figure 29 - Management Interface Signals

Table 20 - Management Interface Signal Definitions

Signal	Direction	Description
SERIAL_DATA	MAC to PHY	For write operations, the MAC drives register address and register data to the PHY
	PHY to MAC	For read operation, the MAC drives register address to the PHY. The PHY drives register data to the MAC
NOTE It is the responsibility of the MAC to ensure the SERIAL_DATA signal is driven to the ZERO level except during READ or WRITE operations.		

11.13.2 Operation of the Management Interface

11.13.2.1Read Operation

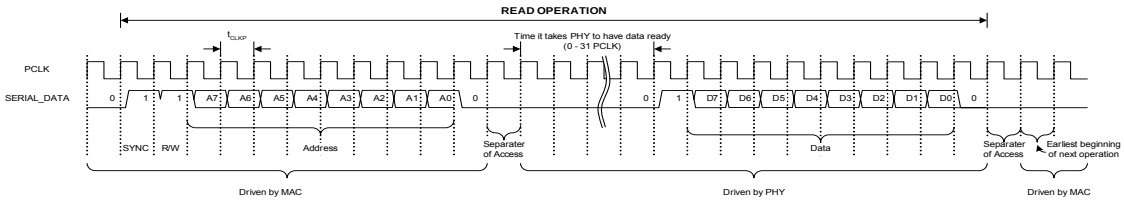

Figure 30 - Serial Read Operation

For a serial read operation, the MAC drives the first part of the transaction, which includes the PHY register address. The PHY drives the second part of the transaction, which includes the requested data. Regardless of whether the MAC or PHY drives the Management Interface, every bit driven on the SERIAL_DATA line is always synchronized with PCLK.

The MAC will drive a ONE as the first bit on the SERIAL_DATA pin. The second bit is a ONE, which indicates a read operation. The MAC drives the next 8 bits, which are the PHY register address. This allows the MAC to address up to 256 PHY configuration registers. After the 8-bit address, the MAC drives a ZERO bit to place the SERIAL_DATA line in a known state.

The PHY drives ZERO to the SERIAL_DATA line for a period from 0 to 31 PCLK cycles beginning on the second PCLK after the MAC stops driving the interface.

The PHY drives a ONE bit to indicate start of data followed by 8 data bits. The transaction is completed by driving a terminating ZERO bit to place the SERIAL_DATA line in a known state before releasing the line to be driven by the MAC.

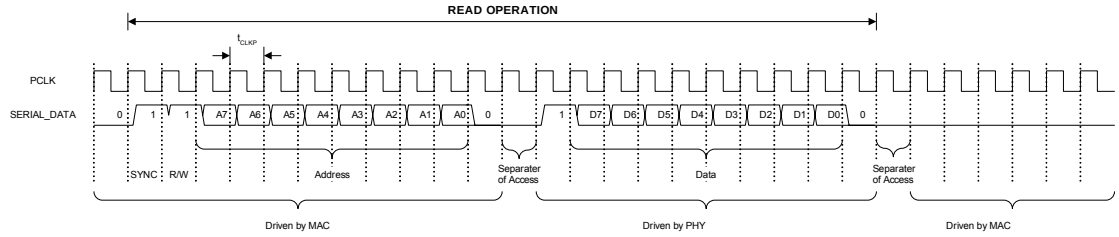

Figure 31 - Fastest Read Response

Figure 31 shows the timing for the fastest PHY response to a read operation.

NOTE
The SERIAL_DATA pin should remain at ZERO when the MAC is no longer driving the signal.

The MAC will resume control of the SERIAL_DATA pin.

11.13.2.2Write Operation

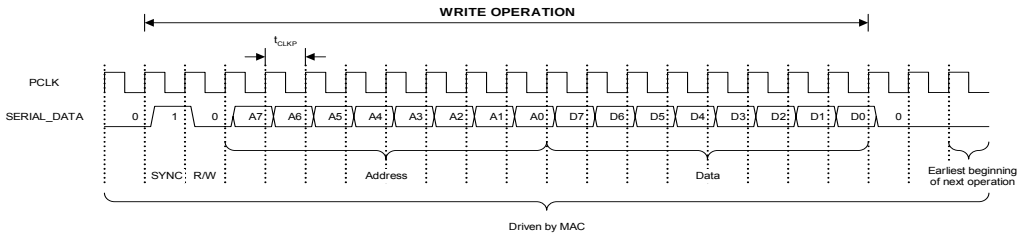

Figure 32 - Serial Write Operation

For a serial write operation, the MAC drives the entire transaction. Each bit the MAC drives on the SERIAL_DATA pin is synchronized with PCLK.

The MAC will drive a ONE as the first bit on the SERIAL_DATA pin. The second bit is a ZERO, which indicates a write operation. The next 8 bits are the PHY address location. This allows the MAC to address up to 256 octets of PHY configuration registers. The next 8 bits are the data to be written to the addressed PHY register. At the end of 8 bits of data, the MAC will drive a terminating ZERO. Once the transaction is complete the MAC stops driving the management interface.

NOTE
The SERIAL_DATA pin should remain at ZERO when the MAC is no longer driving the signal.

The SERIAL_DATA pin will continue to be controlled by the MAC.

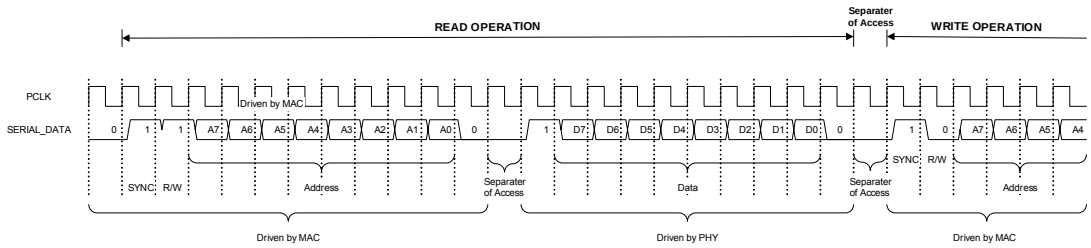

Figure 33 - Read Operation Followed By Write Operation

Figure 33 shows the fastest timing for a read operation followed immediately by a write operation.

11.13.3 Examples

11.13.3.1Read Operation Example

The MAC wants to read the PHYID (addresses 0x20h and 0x21h). PHYID is 1B86 hex stored in big-endian representation. In this example it takes the PHY four clock cycles to have the data available.

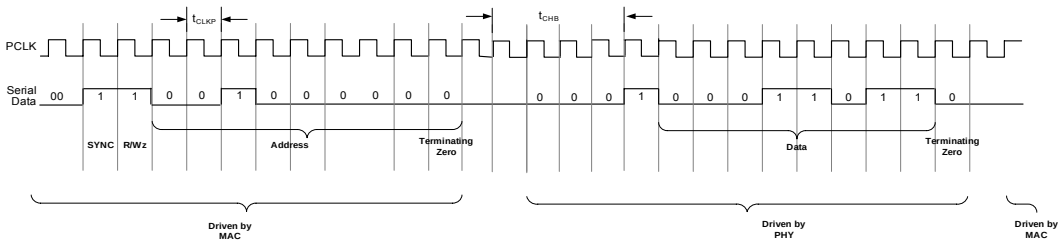

Figure 34 - Serial Read Example, Address 20hex

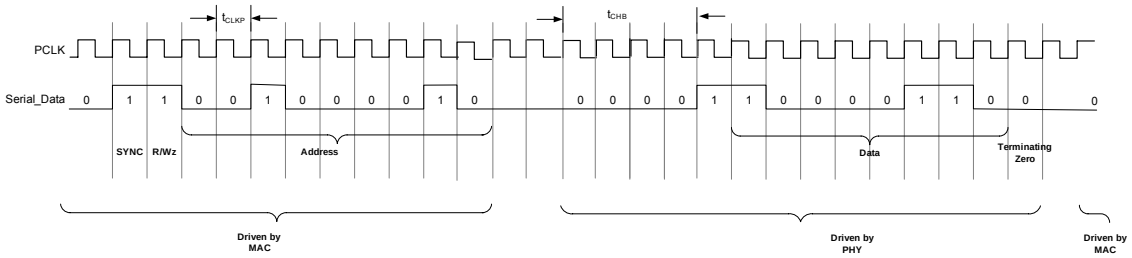

Figure 35 - Serial Read Example, Address 21hex

11.13.3.2Write Operation Example

MAC wants to put PHY into READY state by setting PMMODE=0. (PMMODE address is 06, READY State is value 0.)

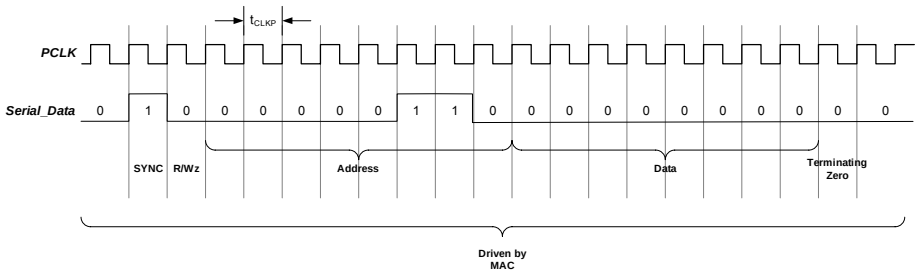

Figure 36 - Serial Write Example Address 06 hex

Annex A
(informative)

Electrical Specifications

A.1 I/O DC Requirements

To improve interoperability between MACs and PHYs from different vendors, the following voltage parameters are recommended:

A.1.1 3,3V DC Specification

Table A.1 gives the Operating Range under nominal parameter values:

- Vcc = 3,0V to 3,6V
- Ambient Temperature = 0^0C to 70^0C

Table A.1 – 3,3V Functional Operating Range

	Parameter	Description	Conditions	Min	Max	Units	Notes
	V_{CC}	Supply Voltage		3,0	3,6	V	
Input	V_{IH}	Input high voltage		2	Vcc+0,5	V	1
	V_{IL}	Input low voltage		-0,3	0,8	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-10	+10	uA	2, 3
	C_{IN}	Input pin capacitance			10	pF	
Output	V_{OH}	Output high voltage	Iout = -4mA	2,4		V	2
	V_{OL}	Output low voltage	Iout = 4mA		0,4	V	2

A.1.2 1,8V DC Specification

Table A.2 gives the Operating Range under nominal parameter values:

- Vcc = 1,65V to 1,95V
- Ambient Temperature = 0^0C to 70^0C

Table A.2 – 1,8V Functional Operating Range

	Parameter	Description	Conditions	Min	Max	Units	Notes
	V_{CC}	Supply Voltage		1,65	1,95	V	
Input	V_{IH}	Input high voltage		1,2	V_{CC}+0,2	V	1
	V_{IL}	Input low voltage		-0,2	0,7	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-600	+600	uA	2, 3
	C_{IN}	Input pin capacitance			2	pF	
Output	V_{OH}	Output high voltage	Iout = -8mA	0,8* V_{CC}	V_{CC}	V	2
	V_{OL}	Output low voltage	Iout = 8mA	0	0,2* V_{CC}	V	2

A.1.3 1,2V DC Specification

Table A.3 gives the Operating Range under nominal parameter values:

- Vcc = 1,1V to 1,3V
- Ambient Temperature = 0^0C to 70^0C

Table A.3 – 1,2V Functional Operating Range

	Parameter	Description	Conditions	Min	Max	Units	Notes
	V_{CC}	Supply Voltage		1,1	1,3	V	
Input	V_{IH}	Input high voltage		0,8	V_{CC} +0,2	V	1
	V_{IL}	Input low voltage		-0,2	0,4	V	1
	I_{IL}	Input leakage current	0 < Vin < Vcc	-120	+120	uA	2, 3
	C_{IN}	Input pin capacitance			2	pF	
Output	V_{OH}	Output high voltage	Iout = -4mA	0,7* V_{CC}	V_{CC}	V	2
	V_{OL}	Output low voltage	Iout = 4mA	0	0,3* V_{CC}	V	2

NOTE 1
This is a DC specification. During transitions the inputs may experience overshoot beyond V_{IH}(max) and undershoot below V_{IL}(min).

NOTE 2
Positive current is defined into the pin.

NOTE 3
Input leakage currents include Hi-Z outputs leakage for bi-directional buffers with tri-state outputs.

A.2 MAC and PHY Timing Specifications

A.2.1 PHY Signal Timing

The following timing for synchronous signals at the PHY is recommended:

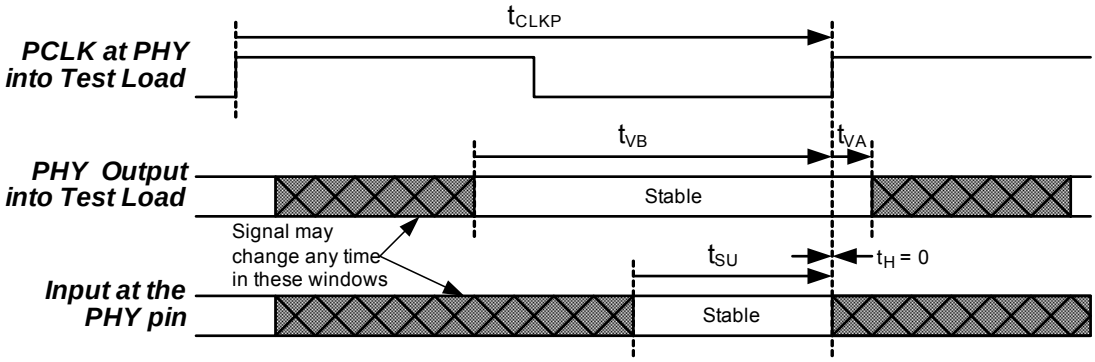

Figure A.1- PHY Signal Timing Diagram

Figure A.1 shows the signal timing for the PHY. Both input and output timing is specified with respect to the rising edge of PCLK driven into the specified test load of 10pF crossing V_{meas} = 1,4V.

Output timing is specified with the PHY pins driven into the specified test load of 10pF, and is measured at V_{meas} = 1,4V.

Input timing is specified at the PHY pin to V_{IL}(max) for a logic ZERO and V_{IH}(min) for logic ONE.

All transitions, except those on !PHY_RESET and STOPC, are synchronous with the rising edge of PCLK.

Table A.4 defines the values for the PHY signal timing requirements.

Table A.4 – PHY Signal Timing Values

Value	Description	Max	Min
t_{CLKP}	PHY Clock Period	-	15ns
t_{VB}	Time PHY output data is valid before the rising edge of PCLK	-	9ns
t_{VA}	Time PHY output data is valid after the rising edge of PCLK	-	1ns
t_{SU}	Setup time, to rising edge of PCLK	-	5ns
t_H	Hold time, from rising edge of PCLK	-	0ns

A.2.2 MAC Signal Timing

The following timing for synchronous signals at the MAC is recommended:

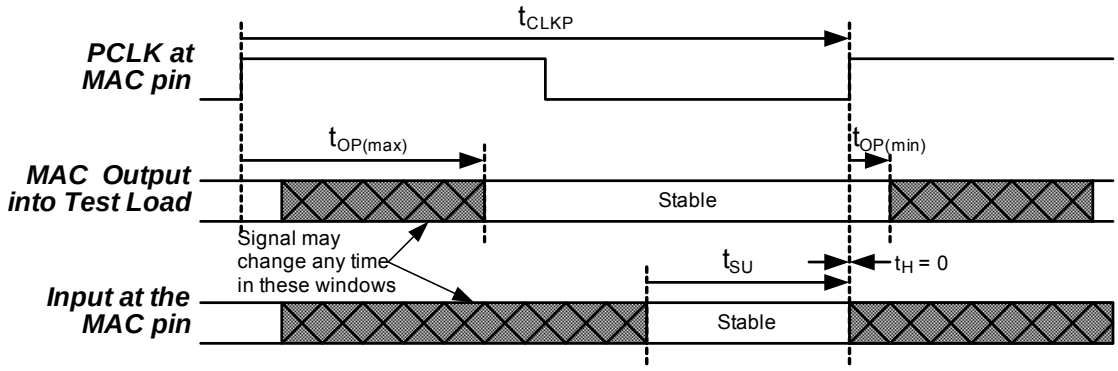

Figure A.2 - MAC Signal Timing Diagram

Figure A.2 shows the signal timing for the MAC. Both input and output timing is specified with respect to rising edge of PCLK at the MAC pin crossing V_{meas} = 1,4V.

Output timing is specified with the MAC pin driven into the specified test load of 10pF, and is measured at V_{meas} = 1,4V.

Input timing is specified at the MAC pin to V_{IL}(max) for a logic ZERO and V_{IH}(min) for logic ONE.

All transitions, except those on !PHY_RESET and STOPC, are synchronous with the rising edge of PCLK.

Table A.5 defines the values for the MAC signal timing requirements.

Table A.5 – MAC Signal Timing Values

Value	Description	Max	Min
t_{CLKP}	PHY Clock Period	-	15ns
t_{OP}	Time MAC output data is valid from the rising edge of PCLK	6ns	1ns
t_{SU}	Setup time, to rising edge of PCLK	-	5ns
t_{H}	Hold time, from rising edge of PCLK	-	0ns

Annex B
(informative)

PHY Vendor and Version Coding

The static parameters defined in 9.3 include two PHY identification parameters – PHYID and PHYVersion. The format and coding of these two variables is defined below. The values for the Vendor ID are found in Annex C of ECMA-368.

B.1 PHYID Format and Coding

Figure B.1 shows the format of the PHYID parameter.

PHYID[15:8]	
Product Code (bits [15:11])	Product Version (bits [10:8])
PHYID[7:0]	
Vendor ID (bits [7:0])	

Figure B.1 - PHYID Format

The first octet of PHYID contains the Vendor ID. The second octet of PHYID contains a 5-bit product code followed by a 3-bit product version number. The coding of product number and version are vendor defined.

B.2 PHY Version Format and Coding

Figure B.2 shows the format of the PHYVersion parameter.

PHYVersion [7:0]	
Major Version Number (bits [7:4])	Minor Version Number (bits [3:0])

Figure B.2 - PHYVersion Format

The PHYVersion parameter contains a 4-bit major version number and a 4-bit minor version number and declares the edition of ECMA-368 to which the PHY implementation complies.