ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-40

HDLC
FRAME STRUCTURE

2nd Edition – September 1976

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ECMA European Computer Manufacturers Association
114 Rue du Rhône — 1204 Geneva (Switzerland)

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BRIEF HISTORY

In March 1970, ECMA received a proposal for a bit-oriented frame structure which was recognized to be an improvement over existing proposals. This new proposal was submitted by TC9 to ISO/TC97/SC6 in 1970.

In June 1972, ISO/TC97/SC6 prepared a proposed Draft International Standard containing the bit-oriented frame structure and other features of high-level data link control (HDLC) and circulated it for voting as ISO DIS 3309.

The first edition of this Standard ECMA-40, in line with the ISO DIS was then published in December 1973.

Subsequently, improvements to the frame checking sequence in DIS 3309 prompted ECMA TC9 to revise the Standard ECMA-40 to align it with the new ISO position. In this occasion, the Standard was editorially revised and information on special conditions and channel states were added. Though not present in ISO DIS 3309, these additions are in line with other ISO DIS on HDLC.

This 2nd Edition of ECMA-40 has been adopted by the General Assembly of ECMA on June 24, 1976.

This 2nd Edition supersedes the Edition issued in December 1973.

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1. SCOPE

This Standard defines in detail the frame structure for bit-oriented High-Level Data Link Control (HDLC). It defines the relative positions of the various components of the basic frame and the bit combination for the frame delimiting sequence (Flag). The bit insertion/deletion mechanism which is used to achieve total transparency within the frame is defined as well as the abort sequence and data channel states. The document also specifies the Frame Checking Sequence (FCS). No details of the encoding of the address and control field are included in this specification. These will be the subject of separate standards.

2. REFERENCE

Standard ECMA-49 HDLC Elements of Procedures.

3. DEFINITIONS

3.1 Data Channel

A one-way digital transmission channel. It includes the transmission media and intervening equipment involved in the transfer of digital data in a given direction.

3.2 Frame

A sequence of bits, transmitted as a unit.

4. FRAME STRUCTURE

The structure of a frame shall be as follows:

- Opening flag
- Address field
- Control field
- Information field, if any
- Frame Check Sequence (FCS)
- Closing flag.

4.1 Frames containing an Information Field

Opening Flag	Address	Control	Information	FCS	Closing Flag
01111110	8 bits	8 bits	see 5.4	16 bits	01111110

frame content

4.2 Frames not containing an Information Field

Opening Flag	Address	Control	FCS	Closing Flag
01111110	8 bits	8 bits	16 bits	01111110

frame content

5. ELEMENTS OF THE FRAME

5.1 Flag

The flag sequence consists of the following bit pattern:

ZERO ONE ONE ONE ONE ONE ONE ZERO

All stations which participate in the data link shall continuously hunt for the flag sequence. The flag is used for frame synchronization. Contiguous frame contents have to be separated by at least one flag. If one flag separates two contiguous frame contents, it acts as closing flag for one frame and opening flag for the next frame.

To avoid simulated flag sequences within the frame content a special transparency mechanism is used (see 7).

5.2 Address Field

The address field shall in all cases identify only the secondary station which is involved in the interchange and, hence, identifies the relationship between the primary and secondary. The address structure is not defined in this Standard and it is application dependent.

5.3 Control Field

The control field is used by the primary to command to the secondary what operation it is to perform. It is also used by the secondary to respond to the primary.

In addition, sequence numbers, where used, are contained in the control field.

5.4 Information Field

Information may be any sequence of bits. In most cases, it will be linked to a convenient character structure, e.g. octets, but, if required, it may be an unspecified number of bits and unrelated to a character structure.

The maximum number of bits to be contained in the information field is application and/or system dependent and it is not specified in this Standard.

5.5 Frame Check Sequence (FCS)

All frames include a 16-bit frame check sequence (FCS) just prior to the closing flag for error detection purpose.

Generation and checking of the FCS is done according to the rules of cyclic coding where:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

is the generating polynomial,

$$P_{k-1}(X) = a_{k-1}X^{k-1} + a_{k-2}X^{k-2} \ldots + a_1X + a_0$$

is the polynomial representation of the k bits of the transmitted frame between, but not including, the final bit of the opening flag and the first bit of the FCS excluding bits inserted for transparency.

5.5.1 FCS generation

At the transmitter, the FCS is calculated as the sum of:

- The remainder of the division (modulo 2) of

  $I(X) = X^k(X^{15} + X^{14} + \ldots + X + 1)$ by $G(X)$.

  Adding (modulo 2) I(X) to the frame contents is equivalent to pre-loading all ONES to the cyclic shift register.

  This is necessary to protect against addition of leading ZERO bits or corrupted leading flag into ZERO bits.

- The remainder of the division (modulo 2) of

  $$X^{16} P_{k-1}(X) \text{ by } G(X).$$

  This corresponds to the normal operation of the cyclic shift register.

- $X^{15} + X^{14} + \ldots + X + 1$, which is equivalent to inverting bit by bit the resulting remainder of the previous divisions.

This FCS is transmitted as the 16-bit sequence with higher order coefficient first, so that the message transmitted is:

$$M(X) = X^{16}P_{k-1}(X) + FCS(X).$$

If errors occur on the link, the message received will be

$$M'(X) = M(X) + E(X)$$

where E(X) represents the error polynomial.

5.5.2 FCS checking

At the receiver, the received frame is checked to detect transmission errors as follows.

The sum of :

- the remainder of the division (modulo 2) of

  $X^{16} \times I(X) = X^{k+16}(X^{15} + X^{14} + \ldots + X + 1)$ by $G(X)$

  [Adding (modulo 2) of $X^{16} \times I(X)$ to the frame content is equivalent to pre-loading all ONES to the cyclic shift register.]

- the remainder of the division (modulo 2) of

  $$X^{16} M'(X) \text{ by } G(X)$$

will be, in the absence of detected errors:

$$X^{12} + X^{11} + X^{10} + X^8 + X^3 + X^2 + X + 1.$$

[The contents of the register are then:

0 0 0 1 1 1 0 1 0 0 0 0 1 1 1 1.]

See Appendix 1 for more details.

6. ORDER OF TRANSMISSION OF FRAME ELEMENTS AND BITS

The elements of the frame shall be transmitted in the following order:

- Opening Flag
- Address Field
- Control Field
- Information Field, if any
- FCS
- Closing Flag

Address and control field shall be transmitted least significant bit first (i.e. the first bit of the sequence number that is transmitted shall have the weight 2^0).

The order of transmitting bits within the information field is not specified by this Standard.

7. FRAME CONTENT TRANSPARENCY

The transmitter shall examine the frame content between the two flag sequences including the address, control and FCS sequences and shall insert a ZERO bit after all sequences of 5 adjacent ONE bits (including the last 5 bits of the FCS) to ensure that a flag, abort or idle sequence is not simulated. The receiver shall examine the frame content and shall discard any ZERO bit which directly follows 5 adjacent ONE bits.

8. SPECIAL CONDITIONS

8.1 Inter Frame Time Fill

Contiguous flag sequences may be used to fill time between frames (see 5.1).

8.2 Idle Sequence

Where required, the idle condition on the receive channel of the data circuit will be indicated to a receiver by means of 15 or more contiguous ONE bits.

8.3 Abort Sequence

Aborting the transmission of a frame is accomplished by transmitting an Abort Sequence, i.e. at least seven contiguous ONE bits (with no inserted ZEROS). Receipt of seven

contiguous ONE bits is interpreted as an Abort and the receiving station will ignore the frame content.

8.4 Invalid Frame

A frame is invalid if it:

- is terminated by an Abort Sequence, or
- contains less than 32 bits (excluding the inserted ZERO bits for transparency; see 7).

The invalid frame must be discarded.

9. DATA CHANNEL STATES

9.1 Active Data Channel State

A Data Channel is considered to enter the Active state when a receiver detects a flag sequence. It will leave that state when 15 contiguous ONE bits are detected.

9.2 Idle Data Channel State

A Data Channel is considered to enter the Idle state when a receiver detects 15 contiguous ONE bits. It will leave that state when a flag sequence is detected.

10. FIELD EXTENSIONS

10.1 Address Field Extensions

Normally a single octet address shall be used and all 256 combinations shall be available. However, by prior agreement the address range can be extended by reserving the first bit of each address octet which would then be set to binary ZERO to indicate that the following octet is an extension of the basic address. The format of the extended octet(s) shall be the same as the basic octet. Thus the address extension may be recursively extended.

When extensions are used, the presence of a binary ONE in the first bit of the basic address octet signals that only one address octet is being used. The use of address extentions thus restricts the range of single octet addresses to 128.

10.2 Control Field Extensions

The control field may be extended by one or more octets. All extensions are subject to further standardization.

APPENDIX I

Background Information on the Equivalent Calculation of the Frame Check Sequence (see 5.5)

1. General

An algebraic notation based on modulo 2 arithmetic is used to describe the FCS generating and checking process. In this notation bit sequences are represented by means of polynomials. For example, bit sequence 1 0 1 0 0 1 0 0 is represented by the polynomial

$$f(X) = X^7 + X^5 + X^2.$$

Note, that the leading bits at the left hand side correspond to the high order coefficients of the polynomial.

It will be supposed that high order coefficients correspond to bits, which are transmitted first.

2. Notations Used

If,

$P_{k-1}(X)$ represents the original message of k bits,

FCS(X) represents the 16-bit frame check sequence, which is transmitted adjacent to the original message, with the higher order coefficient first,

M(X) represents the total message, including the FCS and consisting of k + 16 bits,

then

$$M(X) = X^{16} P_{k-1}(X) + FCS(X).$$

Note, that multiplication of $P_{k-1}(X)$ by X^{16} just creates space for the addition of the frame check sequence FCS(X).

If,

M'(X) represents the message, which is received,

then

$$M'(X) = M(X) + E(X) \qquad (1)$$

where E(X) denotes the polynomial corresponding to the bits in error.

3. Mathematical Equivalence of Inverting a Sequence Bit by Bit

The polynomial expression of a bit sequence of n bits is:

$$R(X) = \sum_{i=0}^{i=n-1} a_i X^i$$

Inverting bit by bit or complementing this bit sequence is equivalent to replace a_i by $\bar{a}_i = 1 + a_i$ (modulo 2). Thus

$$\bar{R}(X) = \sum_{i=0}^{i=n-1} \bar{a}_i X^i = \sum_{i=0}^{i=n-1} (1+a_i)X^i = \sum_{i=0}^{i=n-1} X^i + \sum_{i=0}^{i=n-1} a_i X^i$$

with $L(X) = X^{n-1} + X^{n-2} + \ldots + 1$.

4. FCS Generation

At the transmitter, either the shift register is pre-loaded with all ONES or the 16 high order coefficients of $X^{16} P_k(X)$ are inverted, whereafter modulo 2 division by the generating polynomial G(X) is performed.

In algebraic notation:

$$\frac{X^{16} P_{k-1}(X) + X^k \sum_{n=0}^{15} X^n}{G(X)} = Q(X) + \frac{R(X)}{G(X)}$$

where: $G(X) = X^{16} + X^{12} + X^5 + 1$

$Q(X)$ is the quotient

$R(X)$ is the remainder.

The FCS is the remainder complemented to one, hence

$$FCS(X) = \overline{R(X)} = G(X)\,Q(X) + X^{16} P_{k-1}(X) + (1+X^k) \sum_{n=0}^{15} X^n$$

The bit sequence to be transmitted is given by:

$$M(X) = X^{16} P_{k-1}(X) + FCS$$

or

$$M(X) = G(X)\,Q(X) + (1+X^k) \sum_{n=0}^{15} X^n. \qquad (2)$$

5. FCS Check

At the receiver either the shift register is pre-loaded with all ONES or the 16 high order coefficients of M'(X) are inverted, then the polynomial is multiplied by X^{16}, whereafter modulo 2 division by the generating polynomial is performed.

In algebraic notation, this division can be presented as follows:

$$\frac{(M'(X) + X^k \sum_{n=0}^{15} X^n)\, X^{16}}{G(X)}$$

which, using identities (1) and (2) above, can be rewritten as:

$$X^{16}Q(X) + \frac{X^{16}\,(E(X) + \sum_{n=0}^{15} X^n)}{G(X)}$$

In absence of errors, the unique remainder is the remainder of the division

$$\frac{X^{16} \sum_{n=0}^{15} X^n}{G(X)}$$

This results into $X^{12} + X^{11} + X^{10} + X^8 + X^3 + X^2 + X + 1$, which corresponds to the bit sequence:

0 0 0 1 1 1 0 1 0 0 0 0 1 1 1 1.

APPENDIX 2

Differences between the First and Second Edition

Beside a complete re-editing, with better presentation and distribution of the original contents, there are two main differences between the first and second edition of this Standard ECMA-40.

The first one is in the domain of the Frame Check Sequence (FCS). While the generating polynomial remains the same, the new checking method is based on a new generation and checking of the FCS, in order to protect against errors that would be undetected if flag sequences are garbled. This second edition contains a detailed explanation on the generation and checking of the FCS and an Appendix that gives a complete background information on the FCS calculation.

The second difference consists in the addition of two sections, section 8, Special Conditions, and section 9, Data Channel States. Section 8 contains information on Inter Frame Time Fill, Idle Sequence, Abort Sequence and Invalid Frame. Section 9 contains definitions on Active and Idle Data Channel States. It was felt that the information contained in these two sections was more related to the Frame Structure than to the Elements of Procedure Standard.